HW 4 Solutions

1) Consider a Boolean function $f = gx_2\,x_3 + \overline{x_1}\,\overline{x_2} + x_1\,\overline{x_3}$ where $g = x_4 + x_5$.
Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
Equivalent resistor for an NMOS transistor: R_N**=12kΩ**
Equivalent resistor for a PMOS transistor: R_P**=24kΩ**
Suppose that the output circuit node has a capacitance value of **10pF**. Neglect other internal node capacitors.

Implement ***f*** with "NMOS Pass Transistor Logic – PTL - Network(s)" and "CMOS Inverters" with minimum number of transistors such that there is no threshold voltage drop at the output (output is VDD or GND all the time). For the PTL networks use the ordering of $x_1 - x_2 - x_3 - x_4 - x_5$. Also use only variables $x_1 - x_2 - x_3 - x_4 - x_5$ as inputs, not their negated forms. Find the **minimum number** of transistors needed. Find the **worst case (largest)** t_{PHL} **and** t_{PLH} values (total of 2 values).

$g = x_4(1) + \overline{x_4}(x_5)$

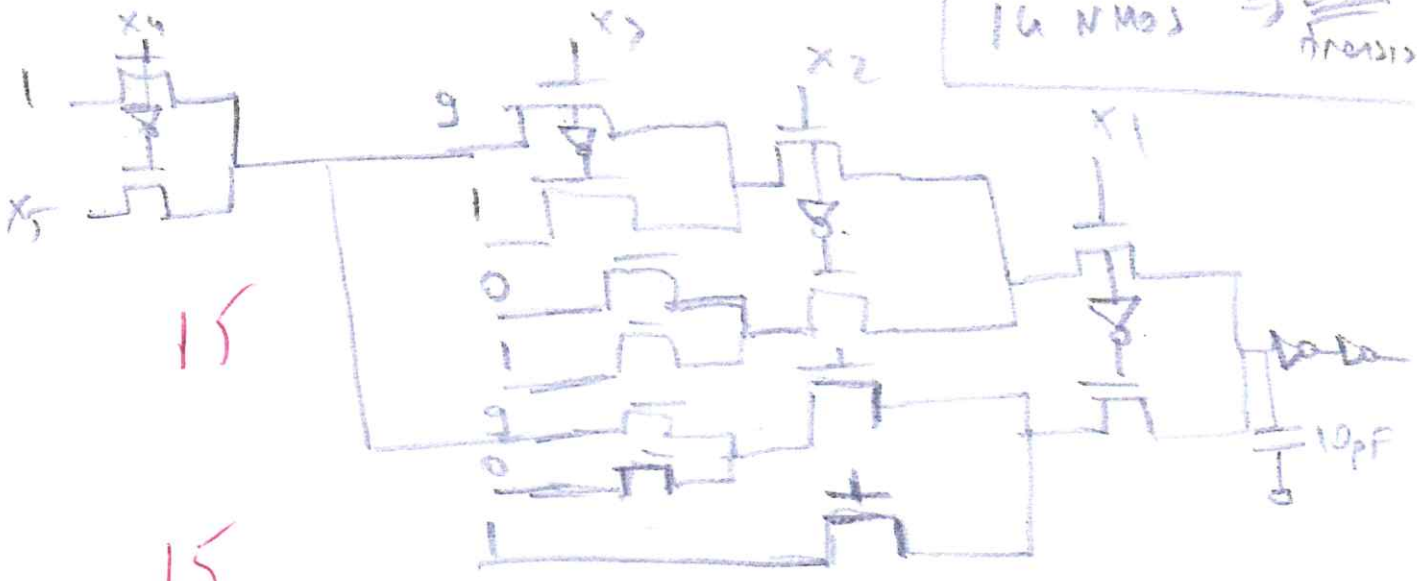
$f = x_1(x_2x_3g + \overline{x_3}) + \overline{x_1}(x_2x_3g + \overline{x_2}) = x_1\left(x_2(x_3g + \overline{x_3}) + \overline{x_2}(\overline{x_3})\right) +$

$= x_1\left(x_2(x_3(g) + \overline{x_3}(1)) + \overline{x_2}(x_3(0) + \overline{x_3}(1))\right) \quad \overline{x_1}\left(x_2(x_3g) + \overline{x_2}(1)\right)$

$+ \overline{x_1}\left(x_2(x_3(g) + \overline{x_3}(0)) + \overline{x_2}(1)\right)$

10

6 inverters
14 NMOS → 26 transistors



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$t_{PHL} \approx t_{PLH} \approx 0{,}69\,(4.12k\;10pF) = 331{,}2\;ns$

2) Consider a Boolean function $f = gx_2\,x_3 + \overline{x_1}\,\overline{x_2} + x_1\,\overline{x_3}$ where $g = x_4 + x_5$. Implement f with "Dynamic Logic" using "Pull-Down NMOS Network(s)" using minimum number of transistors such that there is no charge sharing and cascading problems. Find the **minimum number** of transistors needed.

$$\bar{f} = \bar{g}\,x_2\,x_3 + x_1\,\bar{x}_2\,x_3 + \bar{x}_1\,x_2\,\bar{x}_3$$

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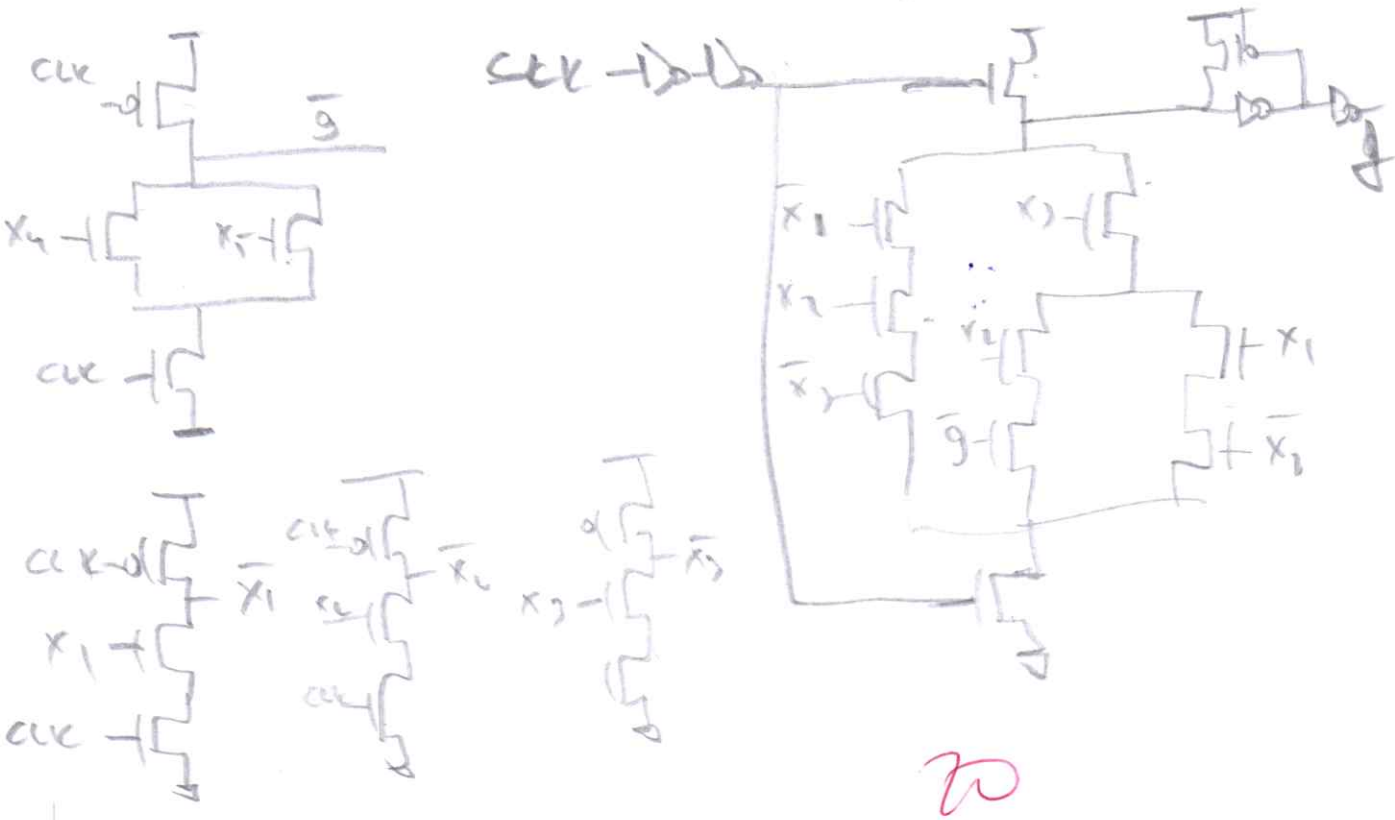
$$= \bar{x}_1\,x_2\,\bar{x}_3 + x_3\,(x_2\,\bar{g} + x_1\,\bar{x}_2)$$



20

8 trans.

4 CMOS Inverters

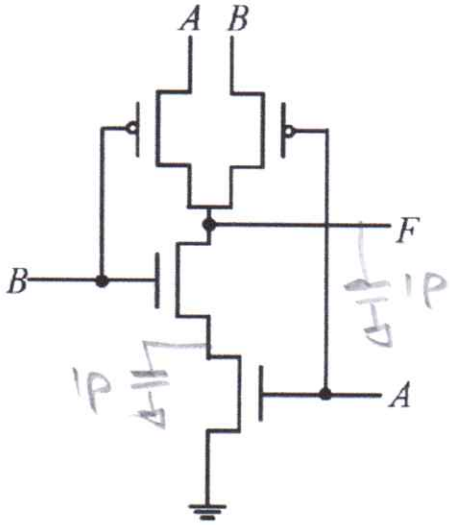
24 other trans.

Total of 32

3) Consider the circuit shown below.

- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
  Equivalent resistor for an NMOS transistor: $R_N = 8k\Omega$
  Equivalent resistor for a PMOS transistor: $R_P = 24k\Omega$
- Suppose that each circuit node (including outputs) has a capacitance value of **1pF**.

a) Derive a Boolean expression for the output ***F*** in terms of the inputs **A** and **B**.
b) Calculate the worst-case and the best-case propagation delays, t_{PLH} and t_{PHL} values (total of 4 values).



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a.)

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

$F = A\bar{B} + \bar{A}B$

5 + 5

b.) $t_{PLH-WC} = t_{PLH-BC} = 0{,}69\,(1P \,||\, 24k) = 16{,}56ns$

$t_{PHL-WC} = 0{,}69\,(16k + 8k\,||\,1P) = 16{,}56ns$ 5

$t_{PHL-BC} = 0{,}69\,((24k\,||\,24k)\,||\,1P) = 8{,}28ns$ 5