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EHB322E Digital Electronic Circuits
QUIZ II

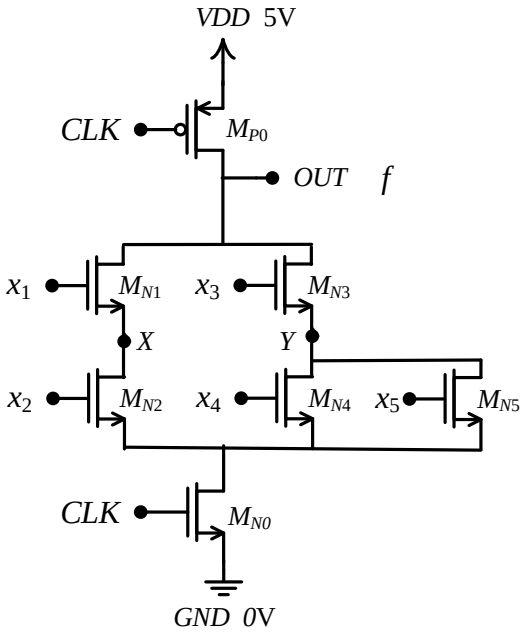
Duration: 60 Minutes

For your answers please use the space provided in the exam sheet

GOOD LUCK!

Consider a dynamic logic circuit shown below.

- Suppose that each transistor has an internal grounded gate capacitor C_G and drain capacitor C_D:
  $C_G = c_{ox}WL$; **$C_D = (c_{ox}WL)/2$**; c_{ox}=1 pF/um^2.
- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
- $W_{N0}=W_{N1}=W_{N2}=W_{N3}==W_{N4}=W_{N5}$=1u, W_{P0}=3u, L=1u, and $V_{TN}=|V_{TP}|$=1V.



Dynamic Logic Circuit

a) Derive a Boolean expression of $\boldsymbol{f}$ in terms of the inputs x_1 through x_5 in evaluation phase.

b) At the start of the evaluation phase suppose that $x_1 = 0 \longrightarrow 1$, $x_2 = 0$, $x_3 = 0 \longrightarrow 1$, $x_4 = 0$, $x_5 = 0$, and V_X = 0V, V_Y = 0V, V_{OUT} = 5V. Considering the charge sharing problem, find the final voltage value at the output.

c) To make the final voltage value at the output as 4.5V, determine the capacitor value of a load to drive.