Homework-2 Solutions – EHB322E

a) • Complex Gate Circuit ① CMOS Logic

$f = x_1 x_2 \bar{x_4} + x_1 \bar{x_2} x_3 + x_2 x_3 \bar{x_4} \rightarrow \bar{\bar{f}} = f \rightarrow f = \overline{\overline{x_1 x_2 \bar{x_4} + x_1 \bar{x_2} x_3 + x_2 x_3 \bar{x_4}}}$

$f = \overline{\bar{x_1} x_2 \bar{x_4} \cdot x_1 \bar{x_2} x_3 \cdot \bar{x_2} \bar{x_3} x_4} = (\bar{x_1} + \bar{x_2} + x_4) \cdot (\bar{x_1} + x_2 + \bar{x_3}) \cdot (\bar{x_2} + \bar{x_3} + x_4)$

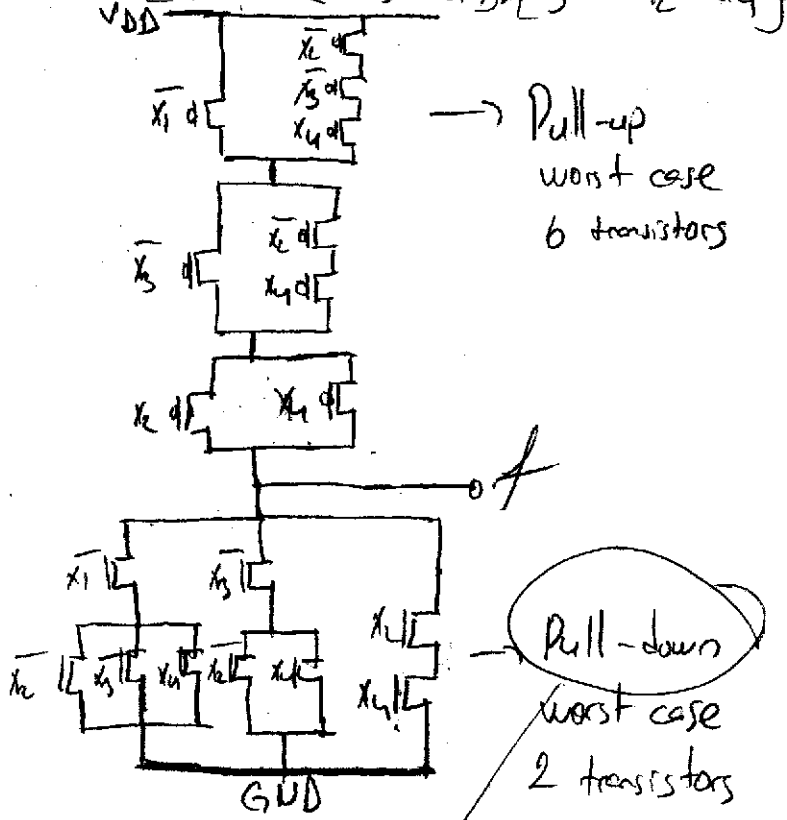
$f = \overline{(\bar{x_1} + \bar{x_2}\bar{x_3} + x_2 x_4 + \bar{x_3} x_4) \cdot (\bar{x_2} + \bar{x_3} + x_4)}$

$f = \overline{\bar{x_1}\bar{x_2} + \bar{x_1}\bar{x_3} + \bar{x_1} x_4 + \bar{x_2}\bar{x_3} + x_2 x_4 + \bar{x_3} x_4} \rightarrow$ for Pull-Down network

$= \bar{x_1}(\bar{x_2} + \bar{x_3} + x_4) + \bar{x_3}(\bar{x_2} + x_4) + x_2 x_4$

⇒ Dual of this expression:

$[\bar{x_1} + (\bar{x_2} \cdot \bar{x_3} \cdot x_4)] \cdot [\bar{x_3} + \bar{x_2} \cdot x_4] \cdot [x_2 + x_4]$



b) $t_{PLH(wc)} = 0.69 \cdot 6.2,6.10^3 \cdot 10.10^{-12}$

$= 107,64$ ns

$t_{PHL(wc)} = 0,69 \cdot (2) \cdot 4,7 \cdot 10^3 \cdot 10 \cdot 10^{-12}$

$= 64,86$ ns

2+1

b)

$t_{PHL} = 0,69 \cdot (3) \cdot 4,7\ 10^3\ 10\ 10^{-12}$

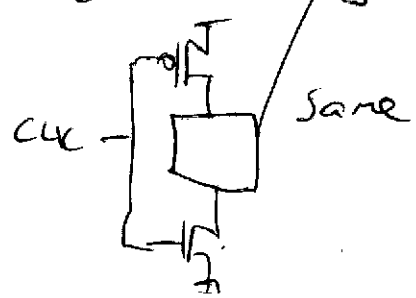
$= 97,29$ ns

$t_{PLH} = 0,69 \cdot (2,6)\ 10^3\ 10\ 10^{-12}$

$= 17,94$ ns (↳ single PMO)

② Dynamic Logic

a)



3) NMOS PTL → $f = x_1 x_2 \bar{x_4} + x_1 \bar{x_2} x_3 + x_2 x_3 \bar{x_4}$

a) Shannon expansion $x_4 \to x_3 \to x_2 \to x_1$

$\Rightarrow x_1 x_2 \bar{x_4}(x_3 + \bar{x_3}) + x_1 \bar{x_2} x_3 (x_4 + \bar{x_4}) + x_2 x_3 \bar{x_4}(x_1 + \bar{x_1})$

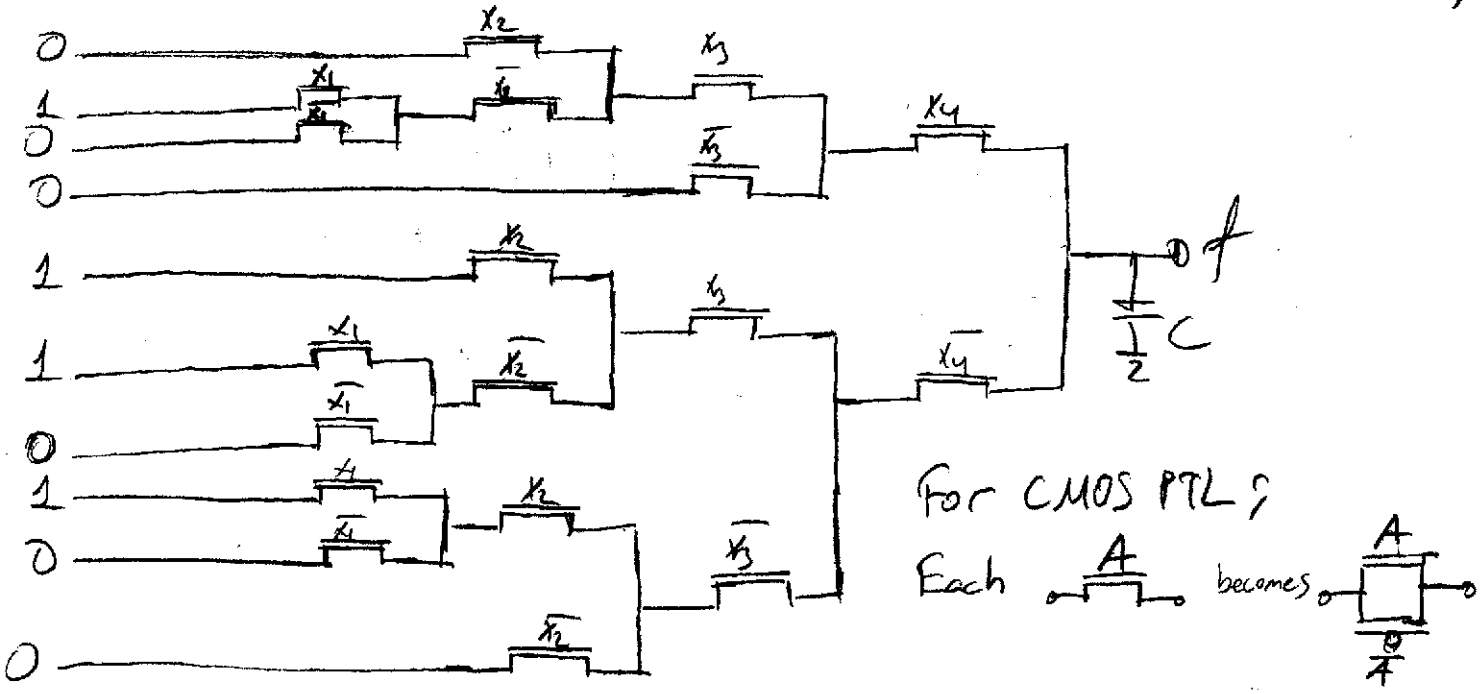
$\Rightarrow x_1 x_2 x_3 \bar{x_4} + x_1 x_2 \bar{x_3} \bar{x_4} + x_1 \bar{x_2} x_3 x_4 + x_1 \bar{x_2} x_3 \bar{x_4} + \cancel{x_1 x_2 x_3 \bar{x_4}} + \bar{x_1} x_2 x_3 \bar{x_4}$

$\Rightarrow x_4 (x_1 \bar{x_2} x_3) + \bar{x_4}(x_1 x_2 x_3 + x_1 x_2 \bar{x_3} + x_1 \bar{x_2} x_3 + \bar{x_1} x_2 x_3)$

$x_4 (x_3 (x_1 \bar{x_2}) + \bar{x_3}(0)) + \bar{x_4}(x_3 (x_1 x_2 + x_1 \bar{x_2} + \bar{x_1} x_2) + \bar{x_3}(x_1 x_2))$

$x_4 (x_3 (x_2(0) + \bar{x_2}(x_1)) + \bar{x_3}(0)) + \bar{x_4}(x_3 (x_2 (x_1 + \bar{x_1}) + \bar{x_2}(x_1)) + \bar{x_3}(x_2(x_1) + \bar{x_2}(0)))$

$x_4 (x_3 (x_2(0) + \bar{x_2}(x_1(1) + \bar{x_1}(0))) + \bar{x_3}(0)) + \bar{x_4}(x_3 (x_2(1) + \bar{x_2}(x_1(1) + \bar{x_1}(0))) + \bar{x_3}(x_2(x_1(1) + \bar{x_1}(0)) + \bar{x_2}(0)))$



b) NMOS PTL → $t_{PLH(WC)} = 0.69 \cdot 4 \cdot R_n \cdot C_{out} = 0.69 \cdot 4 \cdot 4.7 \cdot 10^3 \cdot 10 \cdot 10^{-12}$
$= 129,72\ ns$

↳ 4 transistors on H→L and L→H paths

$t_{PHL(WC)} = 0.69 \cdot 4 \cdot R_n \cdot C_{out} = 129,72\ ns$