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EHB322E Digital Electronic Circuits
MIDTERM I

Duration: 60 Minutes

Grading: 1) 35%, 2) 35%, 3) 30%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

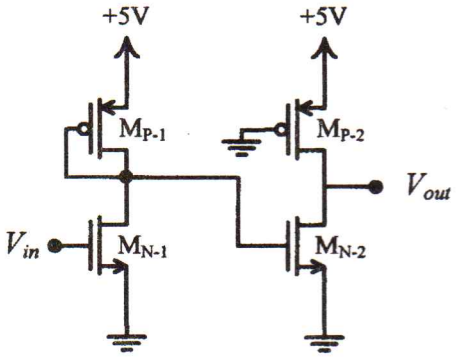
GOOD LUCK!

1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} \left[2(V_{GS} - V_{T0p,n}) V_{DS} - V_{DS}^2 \right]$

Transistor parameters: $k_p' = \mu_p C_{ox} = 35\text{uA/V}^2$, $k_n' = \mu_n C_{ox} = 98\text{uA/V}^2$, $V_{TN} = 1\text{V}$, $V_{TP} = -0.5\text{V}$, $W_{N-1} = 5\text{u}$, $W_{N-2} = 5\text{u}$, $L_P = L_N = 1\text{u}$.



Buffer

a) Find the maximum value of W_{P-1} satisfying that V_{in}=5V results in V_{out}= 5V.

b) Find the value of W_{P-2} if V_{in}=0V results in V_{out}= 1V.

c) Find the buffer's static power consumption values when V_{in}=0V and V_{in}=5V.

10 a) $V_{G,N-1} = 1\text{V} \Rightarrow \frac{1}{2} 98\mu \frac{5}{1} \{2(4).1 - 1^2\} = \frac{1}{2} 35\mu \frac{W_{P-1}}{1\mu} \{4 - 0.5\}^2$

$\Rightarrow W_{P-1} = 8\mu$

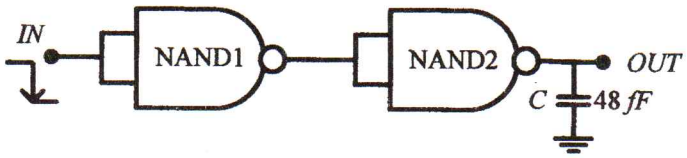
10 b) $V_{G,N-2} = 4.5\text{V} \Rightarrow \frac{1}{2} 98\mu \frac{5}{1} \{2(2.5) 1 - 1\} = \frac{1}{2} 35\mu \frac{W_{P-2}}{1\mu} \{2(4.5) 4 - 4^2\}$

$\Rightarrow W_{P-2} = 4.2\mu$

15 c) $V_{in} = 0\text{V} \Rightarrow I_{total} = I_{DN-2} = 1.47\text{mA}$ $P = 5 \cdot 1.47 = 7.35\text{mW}$

$V_{in} = 5\text{V} \Rightarrow I_{total} = I_{DN-1} = 1.715\text{mA}$ $P = 5 \cdot 1.715 = 8.6\text{mW}$

2) Consider a buffer circuit consisting of two CMOS NAND gates, shown below. An external capacitor of 48*fF* is connected to the output. A signal switching from high to low is applied to the input.
Equivalent resistor for an NMOS transistor: $R_N = (12k\Omega) / (W/L)_N$
Equivalent resistor for a PMOS transistor: $R_P = (24k\Omega) / (W/L)_P$
Gate capacitors $C_{GS\text{-}N} = c_{ox} W_N L_N$ and $C_{GS\text{-}P} = c_{ox} W_P L_P$; neglect C_{GD} capacitors.
Transistor parameters: c_{ox}=1 fF/um2, L_N=L_P=1u, W_{N1}=2u, W_{P1}=3u, W_{N2}=4u, W_{P2}=6u.



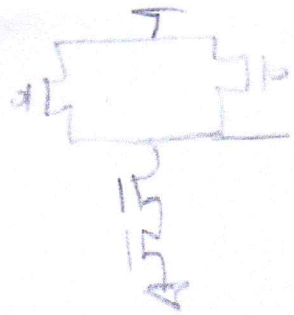
Digital circuit with two CMOS NAND gates

a) Implement a NAND gate with a Boolean function $f = \overline{x_1 x_2}$ using CMOS transistors. If inputs of a NAND gate are shorted, as we use in our circuit, then find its Boolean function. Draw the CMOS implementation of the above circuit.

b) Find the **total propagation delay value** (delay of NAND1 + delay of NAND2) between the input and the output.
- You should consider C_{GS} capacitors as well as the external C=48*fF* capacitor
- Do not consider capacitors at nodes other than the node of gate inputs/outputs.

10

a.)



$f = \overline{x_1 x_2}$ 5

if $x_1 = x_2$ 5//

$f = \overline{x_1}$ → inverter

b.) Output of NAND1 ⇒ $C_1 = (4+6)2\,fF = 20fF$

Output of NAND2 ⇒ $C_2 = C = 48\,fF$ 5//

25

NAND-1	NAND-2
$R_{N-1} = 6k$	$R_{N-2} = 3k$
$R_{P-1} = 8k$	$R_{P-2} = 4k$

5/

total delay = $t_{PLH-1} + t_{PHL-2}$

$= 0.69(R_{P1} // R_{P1} \cdot C_1) + 0.69(R_{N2} + R_{N-2}) C_2$

$= 0.69(4k \cdot 20f + 6k \cdot 48f) = 0.25\,ns$

15// 254 ps //

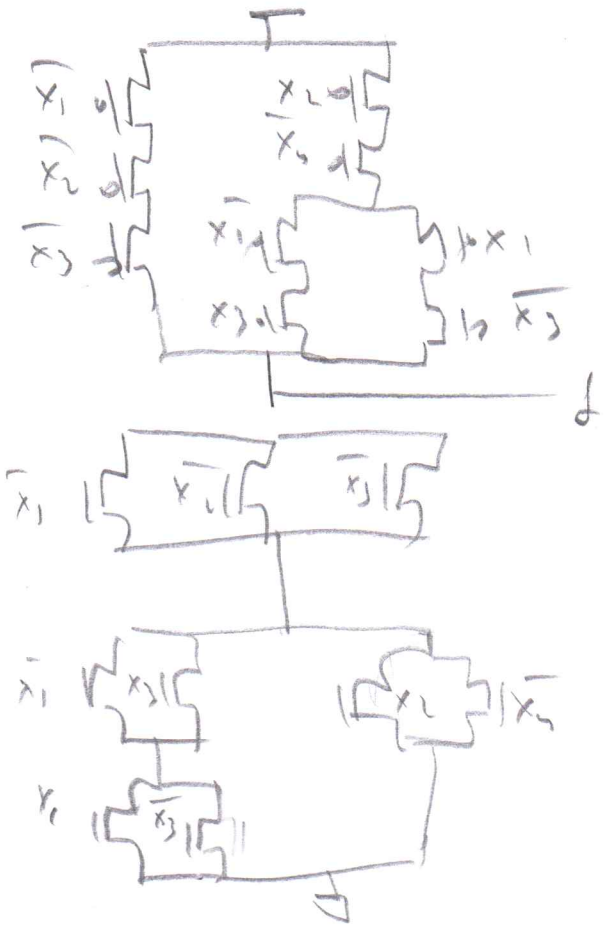
3) Consider $f = x_1x_2x_3 + x_1\overline{x_2}\,\overline{x_3}x_4 + \overline{x_1}\,\overline{x_2}\,x_3x_4$.

a) Implement f with a **CMOS circuit** using **minimum** number of transistors. Draw the circuit. How many PMOS and NMOS transistors do you use?

b) Suppose that both NMOS and PMOS transistors have equivalent resistance values of 1kΩ; a total output load capacitor is 2 *fF* (Neglect all other internal capacitors). Find the **worst case (largest)** t_{PHL} and t_{PLH} values.

a) $f = x_1x_2x_3 + \overline{x_2}x_4(x_1\overline{x_3} + \overline{x_1}x_3)$

9 + 9 = 18 transistors (5)



(5)

b) WC $T_{PLH} = 0,69\,(4\,k)\,2f = 5,52ps$

WC $T_{PHL} = 0,69\,(3\,k)\,2f = 4,14ps$ (5)