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Solutions

EHB322E Digital Electronic Circuits

MIDTERM I

272.00

Duration: 120 Minutes

Grading: 1) 35%, 2) 35%, 3) 30%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

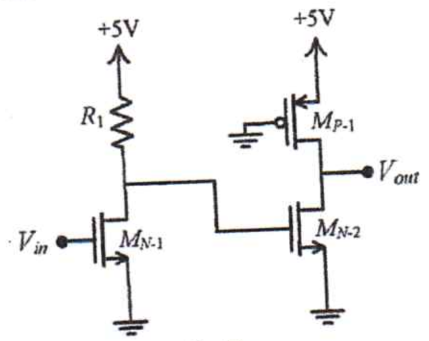
GOOD LUCK!

1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2}k'_{p,n}\frac{W}{L}(V_{GS} - V_{TO\,p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2}k'_{p,n}\frac{W}{L}\left[2(V_{GS} - V_{TO\,p,n})V_{DS} - V_{DS}^2\right]$

Transistor parameters: $k_p' = \mu_p C_{ox} = 54uA/V^2$, $k_n' = \mu_n C_{ox} = 96uA/V^2$, $V_{TN} = 1V$, $V_{TP} = -1V$, $W_{N\text{-}1} = W_{N\text{-}2} = 12u$, $L_P = L_N = 1u$.



Buffer

a) Find the minimum value of R_1 if V_{in}=5V results in V_{out}= 5V.
b) Find the value of $W_{P\text{-}1}$ if V_{in}=0V results in V_{out}= 0.5V.
c) Find the buffer's static power consumption values when V_{in}=0V and V_{in}=5V.
d) Using the values found in a) and b), find the value of V_{out} if V_{in}=2.5V.

10 a) $V_{G2} = 1V \Rightarrow$ M_{N1} is in linear region

$I_{DN\text{-}1} = \frac{1}{2}\, 96\, 12\, [2(4)\,1 - 1] = 4,032\ mA$

$\Rightarrow R_1 = (5V - 1V)/I_{DN\text{-}1} \cong 1k\Omega$

10 b) $V_{G2} = 5V \Rightarrow$ M_{N2} is in linear region
$V_{out} = 0.5V$ $\quad M_{P1}$ is in sat region

$\Rightarrow \underbrace{\frac{1}{2}\, 54\, W_{P\text{-}1}(4)^2}_{I_{DP\text{-}1}} = \underbrace{\frac{1}{2}\, 96\, 12\, [2(4)\,0.5 - 0.25]}_{I_{DN\text{-}2} = 2,16\ mA} \Rightarrow W_{P\text{-}1} = 5\mu$

5 c) $V_{in} = 0V \Rightarrow$ SP $= 2,16 \cdot 5V \cong 10,8\ mW$

$V_{in} = 5V \Rightarrow$ SP $= I_{DN\text{-}1} \cdot 5V \cong 20\ mW$

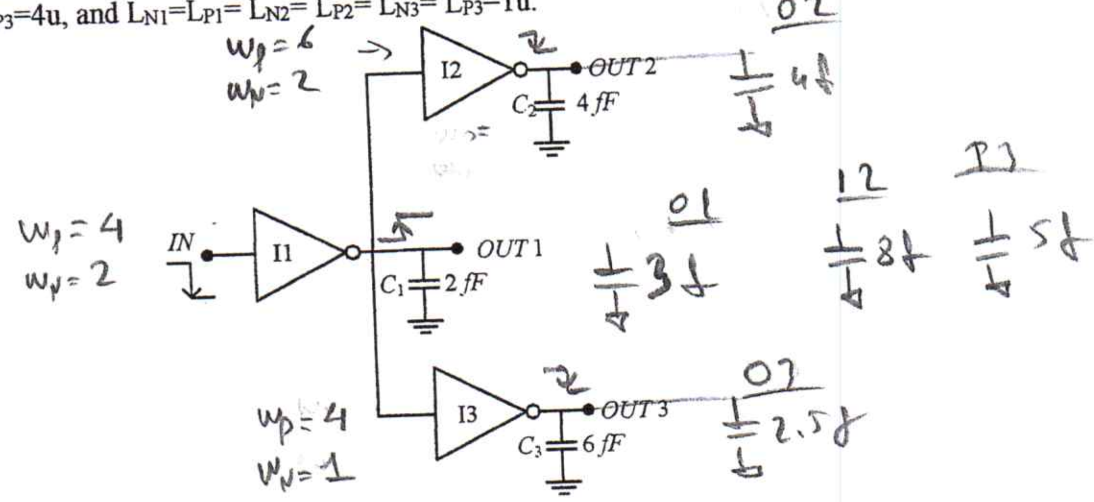
10 d) Suppose that $M_{N\text{-}1}$ is in sat. $\Rightarrow$ Suppose that $M_{P\text{-}1}$ in sat

$I_{DN\text{-}1} = \frac{1}{2}\, 96\, 12\, (1,5)^2 \cong 1,3\ mA \Rightarrow V_{DS\,N\text{-}1} = 3,7V$ Sat ✓

$3,75 = 2,7 \cdot 2 \cdot V_{DS} - V_{DS}^2 \Rightarrow V_{DS} = 0,82$ Sat ✓

$V_{out} = 0,82V$

2) Consider a circuit with three CMOS inverters and three outputs shown below. External capacitors with values of $2fF$, $4fF$, and $6fF$ are connected to output-1, output-2, and output-3, respectively. A signal switching from high to low is applied to the input.
Transistor parameters: c_{ox}=1 fF/um^2, $\tau_n = \tau_p$=1ps, W_{N1}=2u, W_{P1}=4u, W_{N2}=2u, W_{P2}=6u, W_{N3}=1u, W_{P3}=4u, and $L_{N1}=L_{P1}=L_{N2}=L_{P2}=L_{N3}=L_{P3}$=1u.



Digital circuit with three CMOS inverters

Propagation delays of an inverter are formulized as follows. C_L represents the total (internal and external) load capacitor of an inverter.

$t_{PHL} = (C_L/C_N)\,\tau_n$ $\qquad C_N = c_{ox}W_NL_N$

$t_{PLH} = (C_L/C_P)\,\tau_p$ $\qquad C_P = c_{ox}W_PL_P$

Suppose that $C_{GS\text{-}N} = C_N$, $C_{GS\text{-}P} = C_P$, and each inverter has an internal input capacitor of $(C_{GS\text{-}N} + C_{GS\text{-}P})$.

a) Neglect the inverters' internal output capacitors and find **total propagation delay values** at output-1, output-2, and output-3.

b) Suppose that each inverter has an output internal capacitor $C_{I\text{-}out} = c_{ox}(W_N+W_P)(0.5um)$. Find **total propagation delay values** at output-1, output-2, and output-3.

5 for writing t_{PD} equations

a) $t_{PD-1} = t_{PLH1} = \frac{C_L}{C_P}\tau_P$ $\qquad C_L = 2f + 8f + 5f = 15f$, $\quad C_P = 4f$

5 +5 $= 3.75ps$ $\qquad \Rightarrow t_{PD-1} = \frac{13}{4}\,1ps = 3.75ps$

$t_{PD-2} = t_{PLH1} + t_{PHL2}$ $\qquad t_{PHL2} = \frac{C_L}{C_N}\tau_n \Rightarrow t_{PHL2} = 2ps$

5 $= 5.75ps$ $\qquad C_L = 4f \quad C_N = 2f$

$t_{PD-3} = t_{PLH1} + t_{PHL3}$ $\qquad t_{PHL3} = \frac{6}{1}\,ps$

5 $= 9.75ps$

6 for writing the equation

b) 5 $t_{PD-1} = t_{PLH1} = \frac{2+3+8+5}{4}\,ps = 4.5ps$

5 $t_{PD-2} = t_{PLH1} + t_{PHL2} = 4.5p + \frac{8}{2}p = 8.5ps$

5 $t_{PD-1} = t_{PLH1} + t_{PHL3} = 4.5p + \frac{8.5}{1}p = 13ps$

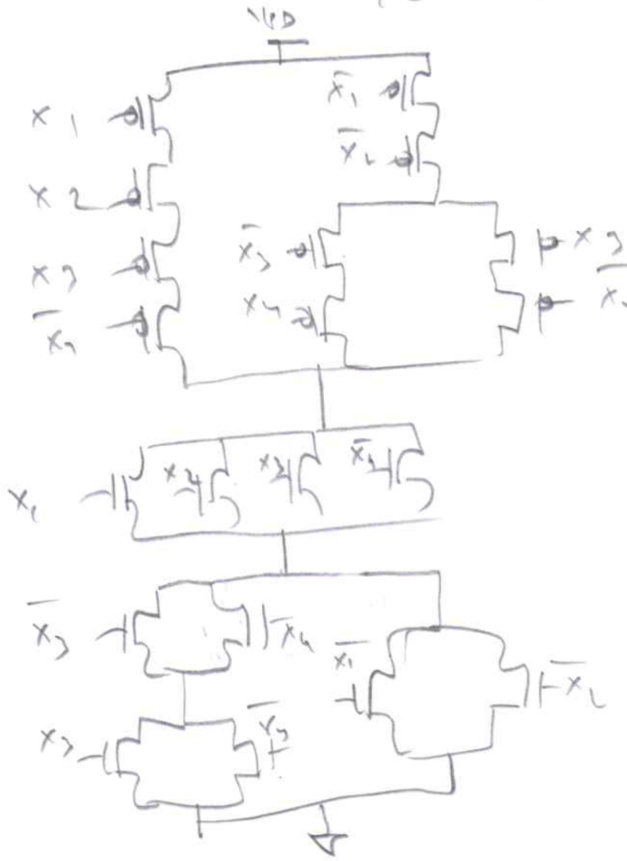
3) Consider $f = x_1x_2x_3\overline{x_4} + x_1x_2\overline{x_3}x_4 + \overline{x_1}\,\overline{x_2}\,\overline{x_3}x_4$.

a) Implement f with a **CMOS circuit** using **minimum** number of transistors. Draw the circuit. How many PMOS and NMOS transistors do you use?

b) Suppose that both NMOS and PMOS transistors have equivalent resistance values of 1kΩ; a total output load capacitor is 2 fF (Neglect all other internal capacitors). Find the **worst case (largest)** t_{PHL} and t_{PLH} values.

a) $f = x_1 x_2 (x_3 \bar{x}_4 + \bar{x}_3 x_4) + \bar{x}_1 \bar{x}_2 \bar{x}_3 x_4$ (10)

10 NMOS 10 PMOS



(10)

b) WC $t_{PHL} = 0{,}69\,(3 \times 1k\Omega)(2f) = 4.14ps$

WC $t_{PLH} = 0{,}69\,(4 \times 1k\Omega)(2f) = 5{,}52\,ps$

(10)