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EHB322E Digital Electronic Circuits
Homework 2

Grading: 1(a)20%, 1(b)20%, 2(a)20%, 2(b)40%

Consider a Boolean function shown below.

$$f = x_1 x_2 \overline{x_4} + x_1 \overline{x_2} x_3 + x_2 x_3 \overline{x_4}$$

1) **CALCULATION:** Use the following parameters for your calculations.
   Equivalent resistor for all NMOS transistors: R_N=4.7kΩ
   Equivalent resistor for all PMOS transistors: R_P=2.6kΩ

   a) Implement ***f*** with "a CMOS Logic Circuit", "an NMOS Pass Transistor Logic Circuit", and "a Dynamic Logic Circuit". For pass transistor logic select an ordering of x_4, x_3, x_2, and x_1. There should be total of **three** circuits/implementations.
   b) Suppose that a load capacitor of 10pF is connected to the output of each circuit (neglect all internal capacitors). Calculate the worst case propagation delays t_{PLH} and t_{PHL} for each implementation. There should be total of **6** delay values.

2) **SIMULATION:** Construct each of the three circuits implemented in **1)-a)** using SPICE. Select V_{DD}=5V (logic 1) and ground=0V (logic 0) for inputs. Connect body terminals of NMOS and PMOS transistor to 0V and 5V, respectively. Select W_P=2u, L_P=1u for all PMOS transistors; select W_N=1u, L_N=1u for all NMOS transistors. Use T15DN and T15DP spice models for NMOS and PMOS transistors, respectively (for details refer to Homework 1).

   a) Statically test your implementations by applying two cases x_1**=1**, x_2**=0**, x_3**=1**, x_4**=1**, and x_1**=0**, x_2**=1**, x_3**=0**, x_4**=1**. For each case sketch V_{OUT} in time domain. There should be total of **6** Spice figures.
   b) Connect a load capacitor of 10pF to the output of each circuit. Apply square pulse waves with frequency of 10kHz to required inputs. Find the worst case propagation delays t_{PLH} and t_{PHL}, by sketching V_{IN} & V_{OUT} in time domain, for each implementation. There should be total of **6** delay values and Spice figures. Compare your results with those in **1)-b)**; justify your answer.