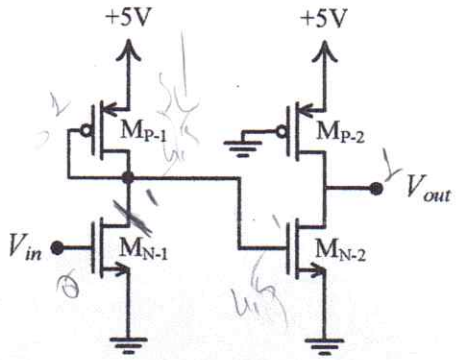
1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} \left[2(V_{GS} - V_{T0p,n}) V_{DS} - V_{DS}^2 \right]$

Transistor parameters: $k_p' = \mu_p C_{ox} = 35\text{uA/V}^2$, $k_n' = \mu_n C_{ox} = 98\text{uA/V}^2$, $V_{TN} = 1\text{V}$, $V_{TP} = -0.5\text{V}$, $W_{N-1} = 5\text{u}$, $W_{N-2} = 5\text{u}$, $L_P = L_N = 1\text{u}$.



Buffer

a) Find the maximum value of W_{P-1} satisfying that V_{in}**=5V** results in V_{out}**= 5V**.

b) Find the value of W_{P-2} if V_{in}**=0V** results in V_{out}**= 1V**.

c) Find the buffer's static power consumption values when V_{in}**=0V** and V_{in}**=5V.**

d) Bu using the W_{P-1} value found in a), find the value of the switching threshold voltage V_M ($V_{in} = V_{GN-2}$) of the first inverter.

10 a.) $V_{6-N-2} = 1\text{V} \Rightarrow \frac{1}{2} 98\mu \frac{5}{1\mu} \{2(4).1 - 1^2\} = \frac{1}{2} 35\mu \frac{W_{p-1}}{1\mu} \{(4-0.5)^2\}$

$\Rightarrow W_{p-1} = 8\mu$

10 b.) $V_{6-N-2} = 4.5\text{V} \Rightarrow \frac{1}{2} 98\mu 5 \{2(2.5) 1 - 1\} = \frac{1}{2} 35\mu \frac{W_{p-2}}{1\mu} \{2(4.5) 4 - 4^2\}$

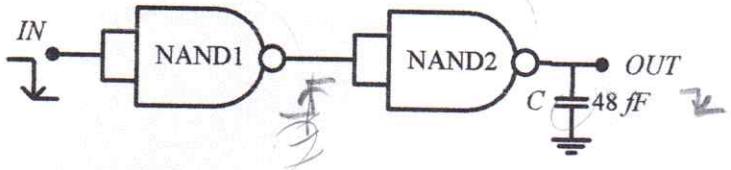
$\Rightarrow W_{p-2} = 4.2\mu$

10 c.) $V_{in} = 0\text{V} \Rightarrow I_{total} = I_{DN-2} = 1,47\text{mA}$ $P = 5\ 1,47 = 7,35\text{m}$

$V_{in} = 5\text{V} \Rightarrow I_{total} = I_{DN-1} = 1,715\text{mA}$ $P = 5\ 1,715 = 8,6\text{mW}$

2) Consider a buffer circuit consisting of two CMOS NAND gates, shown below. An external capacitor of 48*fF* is connected to the output. A signal switching from high to low is applied to the input.

Equivalent resistor for an NMOS transistor: $R_N = (12k\Omega) / (W/L)_N$
Equivalent resistor for a PMOS transistor: $R_P = (24k\Omega) / (W/L)_P$
Gate capacitors $C_{GS\text{-}N} = c_{ox} W_N L_N$ and $C_{GS\text{-}P} = c_{ox} W_P L_P$; neglect C_{GD} capacitors.
Transistor parameters: c_{ox}=1 fF/um2, $L_N = L_P$=1u, W_{N1}=2u, W_{P1}=3u, W_{N2}=4u, W_{P2}=6u.



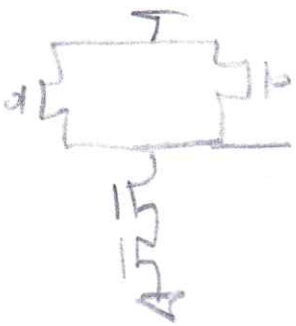
Digital circuit with two CMOS NAND gates

a) Implement NAND gates with a Boolean function $f = \overline{x_1 x_2}$ using CMOS transistors. If inputs of a NAND gates are shorted, as similarly we use in our circuit, then find its Boolean function.

b) Find the **total propagation delay value** between the input and the output.
- You should consider C_{GS} capacitors as well as the external C=48*fF* capacitor
- Do not consider capacitors at nodes other than the node of gate inputs/outputs.

10

a)



$f = \overline{x_1 x_2}$ 5

if $x_1 = x_2$ 5

$f = \overline{x_1}$ → inverter

10

b) Output of NAND1 $\Rightarrow C_1 = (4+6)2\,fF = 20\,fF$

Output of NAND2 $\Rightarrow C_2 = C = 48\,fF$ 5

NAND-1	NAND-2
$R_{N-1} = 6k$	$R_{N-2} = 3k$
$R_{P-1} = 8k$	$R_{P-2} = 4k$

5

total delay $= t_{PLH-1} + t_{PHL-2}$

$= 0.69\left(R_{P1} // R_{P1} \cdot C_1\right) + 0.69\left(\left(R_{N2} + R_{N-1}\right) C_2\right)$

$= 0.69\,(4k \cdot 20f + 6k \cdot 48f) \cong 0.25\,ns$

10 25 pts

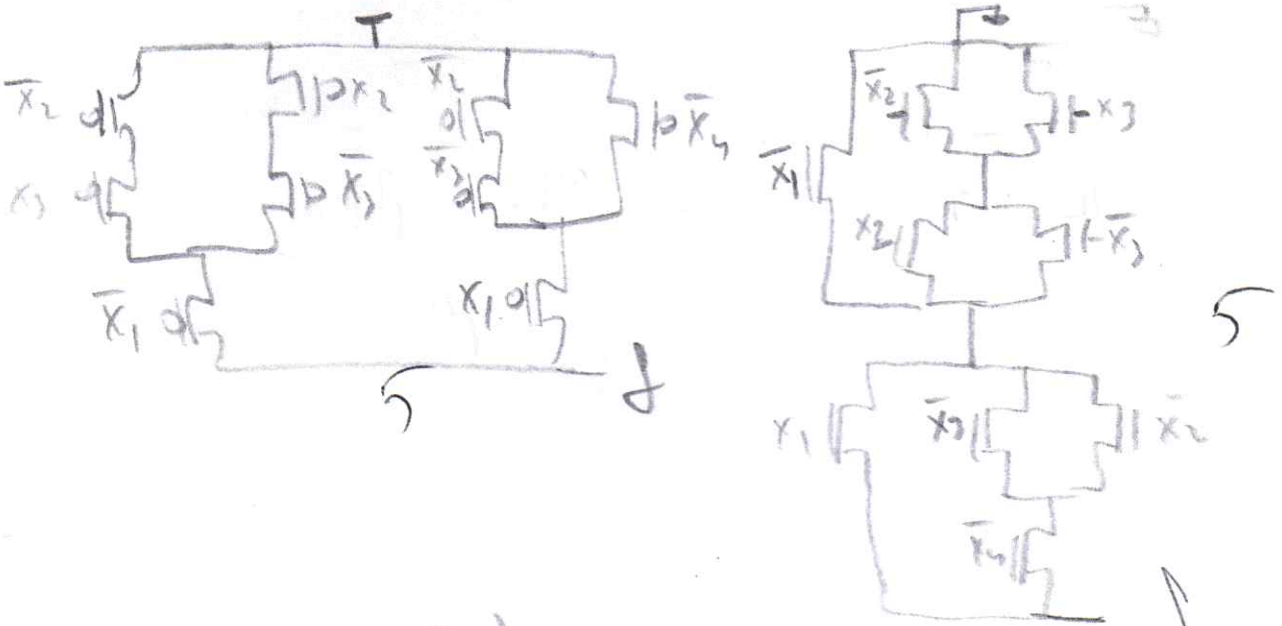
3) For a specific technology and a specific supply voltage, a CMOS inverter with parameters W_P=1u, W_N=1u, L_P=1u, L_N=1u, and a total output load capacitor of 1 *fF* has t_{PHL} =1ns and t_{PLH}=2ns. By considering the same technology and the supply voltage,

a) Implement $f = x_1x_2\overline{x_3} + x_1\overline{x_2}x_3 + \overline{x_1}x_2x_3 + \overline{x_1}x_4$ with a **CMOS circuit** using **minimum** number of transistors. Draw the circuit. How many PMOS and NMOS transistors do you use?

b) Select W_P=4u for all PMOS transistors and W_N=2u for all NMOS transistors of your CMOS circuit. Find the **worst case (largest) and** the **best case (smallest)** t_{PHL} and t_{PLH} values if a total output load capacitor is 2 *fF*. Neglect internal node capacitors. You should report 4 delay values.

20 a) $f = x_1(x_2\overline{x_3} + \overline{x_2}x_3) + \overline{x_1}(x_2x_3 + x_4)$ 10

8 NMOS 8 PMOS → 18 transistors



20 b) t_{PLH} Best → $\alpha \frac{5}{3} R_P$ $x_1=0$ $x_4=1$ $x_2=1$ $x_3=1$

Worst $\alpha 3R_P$ $x_1=0$ $x_4=0$ $x_2=1$ $x_3=1$

t_{PHL} Best $\alpha \frac{13}{6} R_N$ $x_1=0$ $x_2=0$ $x_3=0$ $x_4=0$

Worst $\alpha 3 R_N$ $x_1=1$ $x_2=0$ $x_3=0$ $x_4=1$

BC $t_{PLH} = t_{PLH\text{-in}} \cdot 2\frac{1}{4}\cdot\frac{5}{3} = \frac{5}{3}$ n 5 $t_{PHL} = t_{PHL\text{-in}} \cdot 2\frac{1}{2}\frac{13}{6} = \frac{13}{6}$ n 5

WC $t_{PLH} = 2n \cdot 2\cdot\frac{1}{4}\cdot 3 = 3n$ 5 $t_{PHL} = 1n \cdot 2\frac{1}{2}\cdot 3 = 3n$