

The Level 3 Based SPICE Model for Low-Voltage Pentacene Thin Film Transistors

Nihat Akkan

Electronics and Communication Engineering
Yildiz Technical University
Istanbul, Turkey
nakkan@yildiz.edu.tr

Herman Sedef

Electronics and Communication Eng.
Yildiz Technical University
Istanbul, Turkey
sedef@yildiz.edu.tr

Mustafa Altun

Electronics and Communication Eng.
Istanbul Technical University
Istanbul, Turkey
altunmus@itu.edu.tr

Abstract—A modeling technique is presented for organic thin film transistors (OTFTs) in LTspice platform, using the Level 3 MOSFET model with additional four model parameters. First, the mobility model equation is simplified. Next, the evaluated drain current of the Level 3 model is manipulated proportionally to the recently proposed OTFT mobility model. On the other hand, the model performance is enhanced in the subthreshold regime adding off-state current. This behavioral model is built by using one PMOS transistor and two behavioral current sources. Then, the Level 3 model parameters are obtained fitting the model equations to the low-voltage pentacene-based OTFT data using previously studied metaheuristics-based parameter extraction approach. Finally, the behavioral model based on the Level 3 is simulated in LTspice while the gate and drain voltages are both ranging from 0 to -3 V. It is validated within this range, comparing the experimental and modeled characteristic curves. This model can be more convenient for very large OTFT-based digital circuit simulations.

Index Terms—Organic Thin Film Transistors, Level-3, SPICE, Behavioral modeling, Pentacene

I. INTRODUCTION

Organic thin film transistors have an important role in applications of flexible, light-weight, low-cost, and large-area electronics. There are various researches covering transistor-level and circuit-level investigations that some of them contains thousands of OTFTs [1], [2].

Compact models are necessary to extend transistor-level researches to circuit-level designs and to realize them. In order to predict accurately the electrical behavior of OTFTs and their circuit applications, OTFT-specific accurate compact models are required. However standard, widely accepted SPICE (Simulation Program with Integrated Circuit Emphasis) models are difficult to find due to rapid evolution of organic semiconductors, gate oxides, as well as device structures. There are some papers reporting compact modeling with physical approaches [3]–[7]. Alternatively, some papers have reported adapted models based on inorganic TFT or MOSFET SPICE models [8]–[12]. Meixner *et al.* [8] presented a Pspice model for OTFTs based on the standard BSIM (Berkeley Short-channel IGFET Model) equations. They modified the model

This work was supported by the Research Fund of Yildiz Technical University (Project no. FDK-2018-3477). This work was also supported in part by the Tubitak 1001 under Project #116E250 and the Tubitak-2501 under Project #218E068

equations by additional voltage-controlled current sources to involve the gate voltage dependence of the charge carrier mobility and the bulk conductivity according to their poly(3-hexylthiophene-2,5-diyl) (P3HT)-based OTFTs.

Recently, the Level 3 model has been experienced in our modeling and parameter extraction work [13] for the novel four-terminal switches and in this work, it is adapted for low voltage pentacene-based OTFTs in LTspice [14], a freeware SPICE simulator. The Level 3 model can be more convenient considering the channel dimensions of OTFTs and it has rather less parameters comparing to the BSIM. Here, we contribute to the modeling efforts for OTFTs presenting a method to implement a recently proposed semi-empirical OTFT mobility formulation [15], covering both the subthreshold and above-threshold regimes. Thus, the drain current of Level 3 model can be adapted according to the experimental data of low-voltage pentacene-based OTFTs. First, some inconvenient model parameters of the Level 3 are nullified and mobility term is simplified. Next, the drain current is manipulated proportionally to the OTFT mobility term using a behavioral current source so as to be in agreement with the experimental current-voltage (I-V) data. Off-current is also involved using another behavioral current source. Then, the Level 3 model parameters and the other introduced parameters are extracted using metaheuristics-based optimization algorithms. Finally, the experimental and modeled characteristic curves are compared to show the performance of the presented behavioral model, and thus it is validated.

The organization of the rest of our article is as follows: Section II describes the model and methodology. Next, Section III gives the comparison of the simulation results with the experimental data. Finally, Section IV concludes the article.

II. MODEL DESCRIPTION

A compact model is necessary to use OTFTs for circuit designs in SPICE tools. In this work, we used the Level 3 MOSFET model in LTspice platform. It is a semi-empirical model and developed for transistors having over $1\mu\text{m}$ channel lengths. Despite its many shortcomings, it is relatively simple, robust and computationally more efficient; thus it shows better performance comparing to the previous first generation MOSFET models (*i.e.*, Level 1 and Level 2).

In the Level 3 model, the drain current expression for both linear and saturation regions including channel length modulation is given in [16] as follows:

$$I_{ds} = \frac{\mu_{eff} C_{ox} W_{eff}}{L_{eff} - L'} \times \left\{ (V_{gs} - V_t) V_{ds}' - \frac{V_{ds}'^2}{2} \left[1 + \frac{f_s \gamma}{4(2\phi_f - V_{bs})^{\frac{1}{2}}} + f_n \right] \right\}, \quad (1)$$

where $V_{ds}' = \min(V_{ds}, V_{dsat})$ and μ_{eff} stands for effective mobility; C_{ox} is oxide capacitance; W_{eff} and L_{eff} are respectively effective channel width and length; the distance between drain terminal and pinch-off point is denoted as L' ; V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage, V_{bs} is the bulk to source voltage, V_{dsat} is the drain saturation voltage, and V_t is the threshold voltage; f_s and f_n indicate short channel effects and narrow channel width effects, respectively; γ is the body effect factor and $2\phi_f$ is the surface potential.

The Level 3 has a separate subthreshold current equation based on the model of Swanson and Meindl [17]. The subthreshold current I_{sub} is described in [16] by

$$I_{sub} = I_{on} e^{q(V_{gs} - V_{on})/nkT}. \quad (2)$$

I_{on} represents the drain current when $V_{gs} = V_{on}$. V_{on} is a modified threshold voltage. T is an ambient temperature, q is the charge of an electron, and k is the Boltzmann constant. n can be approximated by (3) because OTFT has no substrate bias.

$$n = 1 + \frac{q NFS}{C_{ox}}, \quad (3)$$

where NFS is the model parameter. It can be considered as an empirical fitting constant and the variations in the subthreshold behavior are related to this parameter.

Mobility model is extremely important to accurately model the device. The Level 3 mobility model covers both the vertical and lateral field effect. These effects are considered to be independent of each other. First the low field mobility μ_0 is taken. Next, it is modified due to the vertical field and μ_v is derived by

$$\mu_v = \left(\frac{\mu_0}{1 + \theta (V_{gs} - V_t)} \right), \quad (4)$$

where θ is the model parameter. Finally, the effective mobility μ_{eff} is derived as given in (5) by modifying μ_v due to lateral field.

$$\mu_{eff} = \left(\frac{\mu_v}{1 + \frac{\mu_v \cdot V_{ds}'}{V_{MAX} \cdot L_{eff}}} \right) \quad (5)$$

In this equation, V_{MAX} is the model parameter and represents the saturation velocity. When the device has a very long channel, the carrier velocity can not reach saturation velocity. In this case V_{MAX} will become an insignificant parameter. If V_{MAX} is set to 0 by a user, μ_{eff} is not directly calculated by (5) and μ_{eff} becomes μ_v . As seen from (4), the vertical field reduces the mobility above threshold voltage. However, the counter examples are observed for OTFTs.

In the first example, a mobility equation is given in [18] by

$$\mu = \mu_0 \left(\frac{V_{gs} - V_t}{V_{AA}} \right)^\gamma, \quad (6)$$

where γ and V_{AA} are model parameters to adjust mobility. In another work [8], mobility is analytically approximated by

$$\mu = \mu_0 - \mu_1 \exp\left(\frac{V_{gs}}{V_{\mu_0}}\right), \quad (7)$$

where μ_1 and V_{μ_0} are model parameters. A semi-empirical mobility model proposed in [15] is the last example given here and it is rewritten for p-type OTFTs as follows:

$$\mu = \frac{\mu_{sub}}{1 + \exp(-m_0 V_{gt})} + \frac{\mu_{ab}}{1 + \exp(m_0 V_{gt})}, \quad (8)$$

where μ_{ab} and μ_{sub} represent the mobilities in above- and sub-threshold regimes, respectively, and m_0 is a positive fitting parameter to connect them; $V_{gt} = V_{gs} - V_t$. Expressions (6), (7), and (8) show that mobility for OTFTs increases with V_{gs} .

In the Level 3, the mobility equation is derived according to MOSFET device physics. When a transistor is simulated using this model, the current will be evaluated by the build-in Level 3 functions with the specified model parameters. Those functions can not be directly manipulated. However, the parameters in the model card can be controlled in a way to serve our purpose.

In order to adapt the Level 3 MOSFET model to the studied low-voltage pentacene-based OTFTs, the following method is proposed:

- (i) Set V_{MAX} to 0 because the OTFT is a large device. Thus, the lateral field effect is nullified and μ_{eff} becomes μ_v .
- (ii) Set θ (*THETA*) to 0. In this way, the vertical field effect is nullified and μ_v becomes μ_0 .
- (iii) Now, the Level 3 model is going to evaluate drain current with respect to μ_0 . Considering (8), the following assumption is done: $I_{ds} \propto \mu_0 \left(\frac{A1}{1 + \exp(-A0 V_{gt})} + \frac{A2}{1 + \exp(A0 V_{gt})} \right)$ where $A0$, $A1$, and $A2$ denote m_0 , μ_{sub}/μ_0 , and μ_{ab}/μ_0 , respectively.
- (iv) Add a behavioral current source and implement the above assumption to manipulate the drain current evaluated by the Level 3 model.
- (v) Add another behavioral current source introducing I_{off} parameter to provide minimum off-state current.
- (vi) Extract the remaining Level 3 model parameters from the OTFT data. A list of the Level 3 model parameters are given in Table I. In this work, metaheuristics-based algorithms [19] are preferred. (1) and (2) are considered for the cost functions.

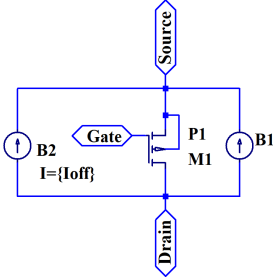
Fig. 1 shows the behavioral model built on LTspice schematic, implementing the method described in this section. In addition, the netlist of this subcircuit is given in Fig. 2.

III. COMPARISON WITH THE EXPERIMENTAL RESULTS

The SPICE model consisting of a PMOS transistor and two behavioral current sources is implemented to model the OTFT data [20]. A PMOS transistor is used with the Level 3 model card to predict I-V characteristics of the OTFT with the help of

TABLE I
THE LEVEL 3 MODEL PARAMETER SET.

Parameter	Units	Description
TOX	m	Thickness of gate oxide
UO	$cm^2/V.s$	Zero bias low field mobility
VTO	V	Threshold voltage for long, wide device under $V_{bs}=0$
GAMMA	$V^{1/2}$	Body factor
PHI	V	Bulk fermi-potential
THETA	V^{-1}	Gate field induced mobility reduction parameter
TPG	—	Type of the gate material
RS	ohm	Source series resistance
RD	ohm	Drain series resistance
LD	m	Lateral diffusion
DELTA	—	Narrow channel effect on the threshold voltage
NSUB	cm^{-3}	Effective substrate doping
XJ	m	Short channel correction to the substrate sensitivity
VMAX	m/s	Maximum carrier velocity
ETA	—	Drain-induced barrier lowering (DIBL) coefficient
KAPPA	V^{-1}	Channel length modulation effect on the drain current
NFS	cm^{-2}	Subthreshold region fitting parameter
CGSO	F/m	Zero bias gate-source capacitance
CGDO	F/m	Zero bias gate-drain capacitance
CGBO	F/m	Zero bias gate-bulk capacitance



For B1:

```
I=Id(M1)*((A1/(1+exp(-A0*(V(Gate, Source)-Vt)))+(A2/(1+exp(A0*(V(Gate, Source)-Vt))))-1)
```

```
.include modelcard.pmos
```

```
.param Leff=10u Weff=100u Ioff=-5e-13 Vt=-1.212 A1=0.134 A2=2.835 A0=1.904
```

Fig. 1. The schematic of the behavioral OTFT model in LTspice. Note that the model parameters are included via ".include modelcard.pmos" command.

two behavioral current sources. These are used for adding off-state current and manipulating the drain current of the Level 3 model to be able to fit it to the OTFT data. In [20], the researchers developed this aforementioned OTFT in bottom-gate top-contact, *i.e.* inverted staggered, device structure with patterned metal gate. Vacuum-deposited pentacene is used as a semiconducting active layer and a thin film of aluminum oxide is used as a gate dielectric material which has a 5.7 nm thickness and provides a gate oxide capacitance per area of $0.7 \mu F/cm^2$. They reported that the device has a channel length and width of $10 \mu m$ and $100 \mu m$, respectively, a carrier mobility of $0.4 cm^2/Vs$, and a threshold voltage of $-1.2 V$.

We have four output characteristic curves of the OTFT, taken by sweeping V_{ds} from 0 to $-3 V$ with steps of $-0.05 V$ when V_{gs} was set to $-1.5 V$, $-2.1 V$, $-2.7 V$, and $-3 V$; two transfer curves of the OTFT, taken by sweeping V_{gs} from 0 to $-3 V$ with steps of $-0.05 V$ when V_{ds} was set to $-0.1 V$ and $-1.5 V$. In order to predict these transistor characteristic curves using the behavioral model given in Fig. 1, the model parameters are extracted running the metaheuristics-based parameter extraction algorithms developed in [19]. A MATLAB script creates the model card including all parameters in the format given in Fig. 3, and then this model card is used in PMOS transistor on schematic shown in Fig. 1 or in netlist of the subcircuit given in Fig. 2. All the model

```
.subckt offt_pentacene Drain Gate Source
M1 Drain Gate Source P1 l={Leff} w={Weff}
B1 Drain Source I=Id(M1)*
+((A1/(1+exp(-A0*(V(Gate, Source)-Vt)))+(A2/(1+exp(A0*(V(Gate, Source)-Vt))))-1)
B2 Drain Source I={Ioff}
.include modelcard.pmos
.param Leff=10u Weff=100u Ioff=-5e-13 Vt=-1.212 A1=0.134 A2=2.835 A0=1.904
.ends offt_pentacene
```

Fig. 2. Netlist for the subcircuit of the presented behavioral OTFT model.

```
.MODEL P1 PMOS LEVEL=3
+TOX = 4.94E-9 U0 = 0.1643 NSUB = 6.88E+16 GAMMA = 0.3695
+PHI = 0.4991 DELTA = 0.5364 TPG = 0
+VMAX = 0 KAPPA = 0.8525 RS = 3.95E+4 RD = 3.95E+4
+NFS = 8.59E+12 ETA=267 THETA=0
+XJ = 7.78E-07 LD = 0
+CGDO = 7.11E-8 CGSO = 7.11E-8 CGBO=0
+CJ = 1.07E-3 MJ = 0.5 PB = 0.4991
```

Fig. 3. Level 3 model card (modelcard.pmos)

parameters used in extraction process are tabulated in Table I. It must be noted that a current value of $G_{min} \times V_{ds}$ is added to the overall drain current of the transistor by LTspice. G_{min} is initially defined as $1E-12$ in LTspice control panel and this parameter causes problems with fitting drain current in the subthreshold regime and decreases accuracy if it is not taken into account. Therefore G_{min} is set as $1E-13$ in the simulations. On the other hand, the off-current parameter I_{off} is fixed to $-5E-13$ using a behavioral current source as shown in Fig.1. Because the off-state drain current is about $0.5 pA$ when $V_{gs} = 0$, as reported in [20]. The oxide thickness is set to $4.94 \times 10^{-9} m$ because effective permittivity of the dielectric material is approximately 4.5. In the Level 3, the gate oxide material is assumed to be silicon dioxide (SiO_2) with $\epsilon_{SiO_2} = 3.9$. Hence, the physical oxide thickness is scaled by $3.9/4.5$. The threshold voltage and the maximum effective mobility values are found as $-1.212 V$ and $0.452 cm^2/Vs$, respectively, and these values are very close to the ones given in [20]. The additional parameters of $A0$, $A1$, and $A2$ are found as 1.904, 0.134, and 2.835, respectively. This additional parameters give us mobility values for the subthreshold and the above-threshold regimes. $\mu_{sub} = 0.022 cm^2/Vs$ and $\mu_{ab} = 0.466 cm^2/Vs$. In the following step, DC simulations of the behavioral model in LTspice platform are performed according to the sweeping conditions of the experimental data. The simulation data is exported from LTspice to a text file. Then, the experimental and simulated model data are compared plotting both of them using a MATLAB script. Fig. 4 gives the modeled transfer characteristic curves in agreement with the experimental data and Fig.5 gives the comparison of output characteristic curves. As seen in these figures, the model shows a satisfying performance. However, it is not very scalable for all device geometries and model binning is almost always required. Transient simulations are not given in this preliminary work due to the page limit; however, the parasitic capacitance parameters are at least included in the model card.

IV. CONCLUSION

In conclusion, a modeling technique is proposed to predict characteristic curves of low-voltage pentacene-based OTFTs,

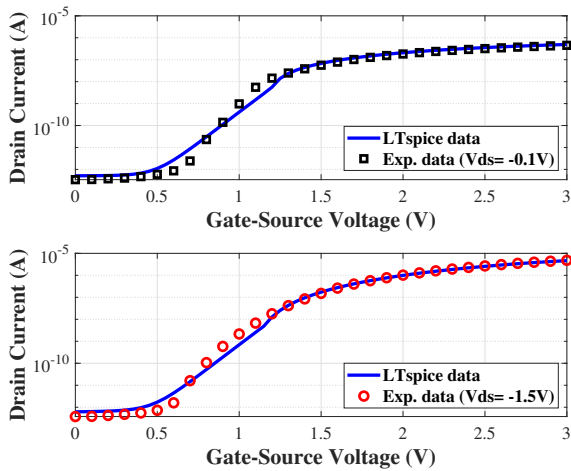


Fig. 4. Comparison of the experimental and modeled transfer characteristics of the OTFT for $V_{ds} = -0.1$ V and -1.5 V.

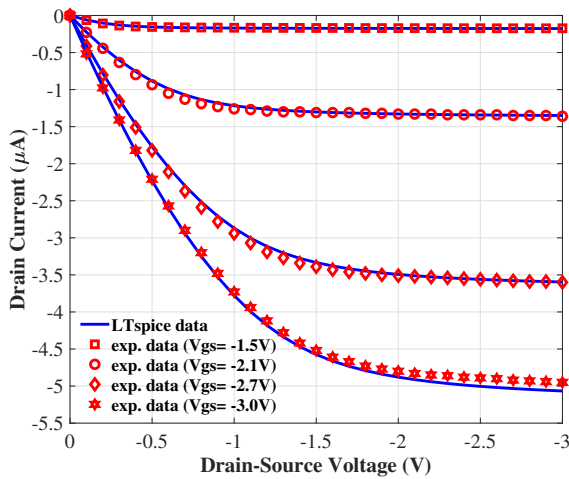


Fig. 5. Comparison of the experimental and modeled output characteristics of the OTFT for $V_{gs} = -1.5$ V, -2.1 V, -2.7 V, and -3 V.

building a behavioral model in LTSpice. The model involves a PMOS transistor including the Level 3 model parameters and two behavioral current sources introducing additional four parameters which help adapting DC I-V curves of the Level 3 model to the characteristic curves of the studied OTFTs. The model data agree well with the experimental transfer and output characteristics data while the gate and drain voltages are both ranging from 0 to -3 V. Therefore, the presented behavioral model shows a satisfying performance. However, the model can be more convenient for very large OTFT-based digital circuit simulations comparing to analog ones, as it is suggested for the Level 3 MOSFET model too. Because it shows a poor output conductance and has a weak subthreshold current model. In future works, the model's transient simulation performance shall be investigated. Besides, it is also necessary to test and specify limitations of this kind of behavioral models for other OTFTs with different organic semiconductors and gate dielectrics. These models can be very practical and helpful in early development phases of the circuit-level designs and realization of them.

REFERENCES

- [1] K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8-Bit, 40-Instructions-Per-Second Organic Microprocessor on Plastic Foil," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 284–291, 2012.
- [2] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuisen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw, "A 13.56-MHz RFID System Based on Organic Transponders," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 84–92, 2007.
- [3] O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, "Organic Thin-Film Transistors: Part I—Compact DC Modeling," *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 2952–2961, 2009.
- [4] M. Estrada, A. Cerdeira, J. Puigdollers, L. Reséndiz, J. Pallares, L. Marsal, C. Voz, and B. Iñiguez, "Accurate modeling and parameter extraction method for organic TFTs," *Solid-State Electronics*, vol. 49, no. 6, pp. 1009–1016, 2005.
- [5] M. Estrada, I. Mejía, A. Cerdeira, J. Pallares, L. Marsal, and B. Iñiguez, "Mobility model for compact device modeling of OTFTs made with different materials," *Solid-State Electronics*, vol. 52, no. 5, pp. 787–794, 2008.
- [6] L. Li, M. Debucquoy, J. Genoe, and P. Heremans, "A compact model for polycrystalline pentacene thin-film transistor," *Journal of Applied Physics*, vol. 107, no. 2, p. 024519, 2010.
- [7] B. Iñiguez, R. Picos, D. Veksler, A. Koudymov, M. S. Shur, T. Ytterdal, and W. Jackson, "Universal compact model for long- and short-channel Thin-Film Transistors," *Solid-State Electronics*, vol. 52, no. 3, pp. 400–405, 2008, Special Issue: Papers Selected from the 3rd International TFT Conference - ITC'07.
- [8] R. M. Meixner, H. H. Gobel, H. Qiu, C. Ucurum, W. Klix, R. Stenzel, F. A. Yildirim, W. Bauhofer, and W. H. Krautschneider, "A Physical-Based SPICE Compact Model for Poly(3-hexylthiophene) Organic Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 55, no. 7, pp. 1776–1781, 2008.
- [9] V. Vaidya, J. Kim, J. N. Haddock, B. Kippelen, and D. Wilson, "SPICE Optimization of Organic FET Models Using Charge Transport Elements," *IEEE Transactions on Electron Devices*, vol. 56, no. 1, pp. 38–42, 2009.
- [10] A. Valletta, A. S. Demirkol, G. Maira, M. Frasca, V. Vinciguerra, L. G. Occhipinti, L. Fortuna, L. Mariucci, and G. Fortunato, "A Compact SPICE Model for Organic TFTs and Applications to Logic Circuit Design," *IEEE Transactions on Nanotechnology*, vol. 15, no. 5, pp. 754–761, 2016.
- [11] O. Yaghamzadeh, Y. Bonnassieux, A. Saboundji, B. Geffroy, D. Tondelier, and G. Horowitz, "A SPICE-like DC Model for Organic Thin-Film Transistors," *Journal of Korean Physical Society*, vol. 54, no. 925, p. 523, Jan. 2009.
- [12] K. Kandpal and N. Gupta, "Adaptation of a compact SPICE level 3 model for oxide thin-film transistors," *Journal of Computational Electronics*, vol. 18, pp. 1–8, 09 2019.
- [13] N. Akkan, S. Safaltin, L. Aksoy, I. Cevik, H. Sedef, C. A. Moritz, and M. Altun, "Technology Development and Modeling of Switching Lattices Using Square and H Shaped Four-Terminal Switches," *IEEE Transactions on Emerging Topics in Computing*, vol. 10, no. 1, pp. 351–360, 2022.
- [14] LTSpice Simulation Software. www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html. (accessed: 03-10-2022).
- [15] N. Li, W. Deng, W. Wu, Z. Luo, and J. Huang, "A Mobility Model Considering Temperature and Contact Resistance in Organic Thin-Film Transistors," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 189–194, 2020.
- [16] D. P. Foty, *MOSFET Modeling with SPICE: Principles and Practice*. Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1997.
- [17] R. Swanson and J. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," *IEEE Journal of Solid-State Circuits*, vol. 7, no. 2, pp. 146–153, 1972.
- [18] A. Cerdeira, M. Estrada, R. Garcia, A. Ortiz-Conde, and F. G. Sanchez, "New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions," *Solid-State Electronics*, vol. 45, no. 7, pp. 1077 – 1080, 2001.
- [19] N. Akkan, M. Altun, and H. Sedef, "Modeling and Parameter Extraction of OFET Compact Models Using Metaheuristics-Based Approach," *IEEE Access*, vol. 7, pp. 180 438–180 450, Dec. 2019.
- [20] H. Klauk, U. Zschieschang, and M. Halik, "Low-voltage organic thin-film transistors with large transconductance," *Journal of Applied Physics*, vol. 102, no. 7, p. 074514, 2007.