

Student Name:

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Student ID:

EHB205E Introduction to Logic Design

Homework 3

Deadline: 27/12/2019 (submit to the TA Emre Altuner before 12:30)

- 1) We will design a circuit called half adder (HA) which adds two 1-bit numbers, a,b and produces 2-bit output, c.
 - a. Draw the truth table of the circuit.
 - b. Find the Boolean functions of each bit of the output.
 - c. Optimize the Boolean functions.
 - d. Draw the logic diagram of the optimized circuits.
 - e. Write the VHDL code of the logic diagrams by using “Dataflow modeling” method using the example given in

<https://tr.scribd.com/doc/118480007/VHDL-Code-for-Half-Adder-by-Data-Flow-Modelling>

<https://steemit.com/vhdl/@drifter1/logic-design-vhdl-behavioral-dataflow-and-structural-models>

https://www.academia.edu/1492361/VHDL_BASICIS_WITH_EXAMPLES

<https://www.slideshare.net/PadmanabanKalyanaram/data-flow-modeling>

- f. Simulate the circuits that you have designed in 1.e. Prepare a simulation waveform for you report.
 - g. Produce the RTL schematic for the circuit that you have designed in 1.e.
- 2) We will design a circuit called full adder (FA) which adds three 1-bit numbers, a,b,c and produces 2-bit output, d.
 - a. Draw the truth table of the circuit.
 - b. Find the Boolean functions of each bit of the output.
 - c. Optimize the Boolean functions.
 - d. Draw the logic diagram of the optimized circuits.
 - e. Write the VHDL code of the logic diagrams by using “Dataflow modeling” method using the example given in

<https://tr.scribd.com/doc/118480007/VHDL-Code-for-Half-Adder-by-Data-Flow-Modelling>

<https://steemit.com/vhdl/@drifter1/logic-design-vhdl-behavioral-dataflow-and-structural-models>

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<https://www.slideshare.net/PadmanabanKalyanaram/data-flow-modeling>

- f. Simulate the circuits that you have designed in 2.e. Prepare a simulation waveform for you report.
 - g. Produce the RTL schematic for the circuit that you have designed in 2.e.

References

- 1) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog**, Hoboken, NJ : John Wiley, 2010.
- 2) [Perry, Douglas L.](#), **VHDL**, New York : McGraw-Hill, c1991
- 3) Botros, Nazeih, **HDL with digital design : VHDL and Verilog**, Dulles, Virginia : Mercury Learning and Information, [2015]
- 4) Vahid, Frank, **VHDL for digital design**, Hoboken, N.J. : Wiley, c2007
- 5) [Short, Kenneth L.](#), **VHDL for engineers**, Upper Saddle River, NJ : Pearson Prentice Hall, c2009
- 6) [Coelho, David R.](#), **The VHDL Handbook**, Boston, MA : Springer US, 1989
- 7) [Lipsett, Roger.](#), **VHDL: Hardware Description and Design**, Boston, MA : Springer US, 1989