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EHB205E Introduction to Logic Design
MIDTERM II

Duration: 120 Minutes

Grading: 1) 20%, 2) 20%, 3) 25%, 4) 35%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

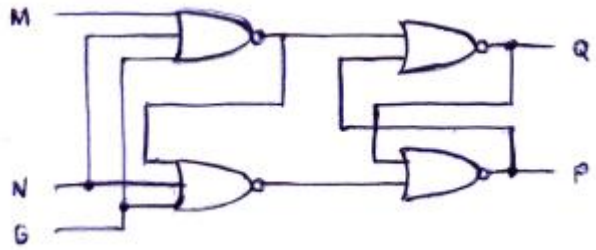
GOOD LUCK!

1) Consider Boolean functions $f_1(x_1, x_2, x_3) = \sum(0,1,3,5,6,7)$ and $f_2(x_4, x_5, x_6) = \sum(2,3,4,5,6,7)$. Implement $f = f_1 + f_2$ using **two 3-to-8 decoders** and minimal number of **two-input NOR gates.**

2) Consider a **6-to-1 multiplexer** having inputs I_0, I_1, I_2, I_3, I_4, I_5; select input S_0, S_1, S_2; and the output OUT.
If $(S_0,S_1,S_2) = (0,0,0)$ then OUT= I_0;
If $(S_0,S_1,S_2) = (0,0,1)$ then OUT= I_1;
If $(S_0,S_1,S_2) = (0,1,0)$ then OUT= I_2;
If $(S_0,S_1,S_2) = (0,1,1)$ then OUT= I_3;
If $(S_0,S_1,S_2) = (1,0,0)$ then OUT= I_4;
If $(S_0,S_1,S_2) = (1,0,1)$ then OUT= I_5.

Implement this 6-to-1 multiplexer multiplier using **minimal number of 2-to-1 multiplexers**.

3) Consider a sequential circuit shown below.



a) For which input values of M, N, and G, **outputs P and Q hold their previous values**?

b) Obtain a minimal sum-of-products **(SOP) expressions for P and Q** in terms of M, N, and G as well as the previous values of P and Q.

4) Consider a flip-flop consisting of four NAND gates, shown below. Suppose that each of the NAND gates has a delay of **2ns**. Suppose that initial values of Q and Q′ are 0 and 1, respectively. Sketch the **waveforms at the outputs Q and Q′** if the input signals A and CLK shown below are applied.