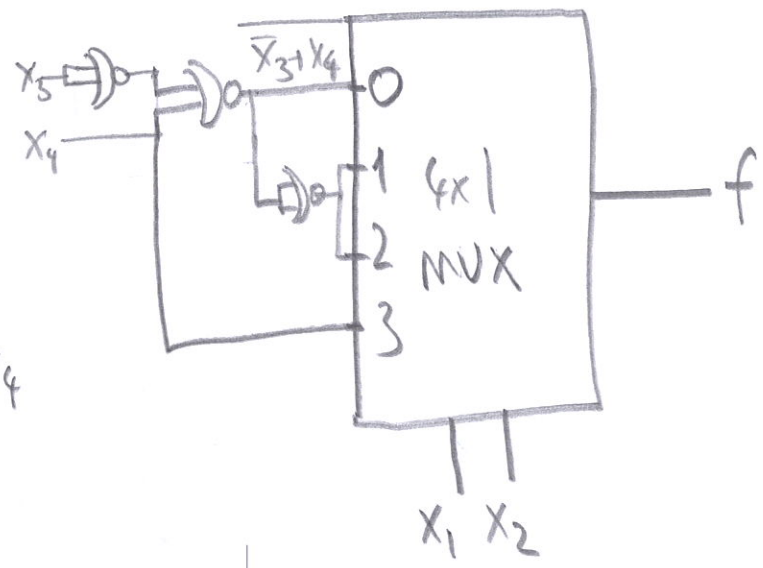
Solutions

1. Implement a 4-variable Boolean function $f(x_1, x_2, x_3, x_4) = \sum(2,4,5,7,8,9,11,13,15)$ using **a single 4-to-1 multiplexer** and minimal number of **two-input NOR gates.** Use x_1 and x_2 as select input lines in the multiplexer. Use only variables x_1, x_2, x_3, x_4 as inputs (**not their negated forms**).

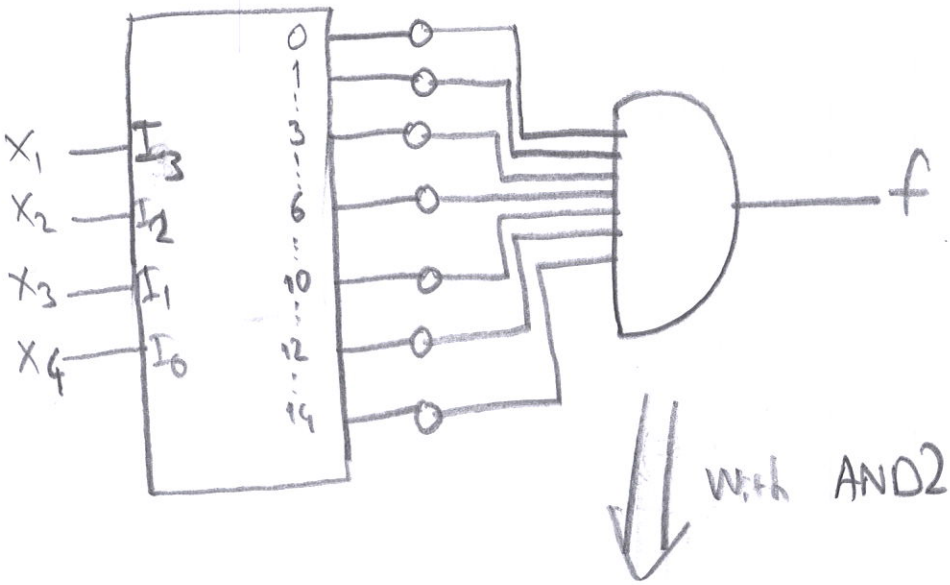
X_1	X_2	X_3	X_4	f	
0	0	0	0	0	$X_3 \cdot \bar{X}_4 = \overline{\bar{X}_3 + X_4}$
0	0	0	1	0	
0	0	1	0	1	
0	0	1	1	0	
0	1	0	0	1	$\overline{X_3 \cdot \bar{X}_4} = \bar{X}_3 + X_4$
0	1	0	1	1	
0	1	1	0	0	
0	1	1	1	1	
1	0	0	0	1	$\overline{X_3 \cdot \bar{X}_4} = \bar{X}_3 + X_4$
1	0	0	1	1	
1	0	1	0	0	
1	0	1	1	1	
1	1	0	0	0	X_4
1	1	0	1	1	
1	1	1	0	0	
1	1	1	1	1	



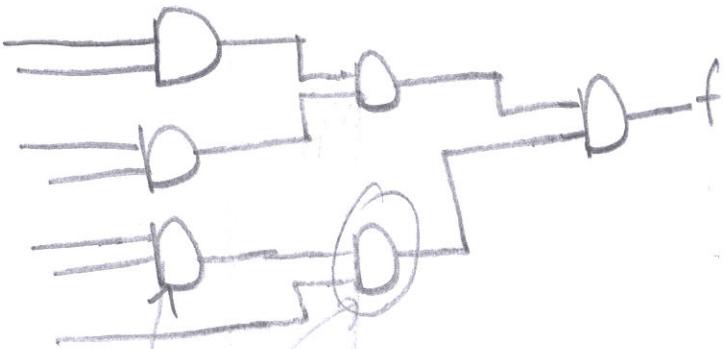
3- OR gates

2. Implement a 4-variable Boolean function $f(x_1, x_2, x_3, x_4) = \sum(2,4,5,7,8,9,11,13,15)$ using **a single decoder** and minimal number of **two-input NAND gates.** Use only variables x_1, x_2, x_3, x_4 as inputs (**not their negated forms**).

$\Sigma = (2,4,5,7,8,9,11,13,15) = \Pi(0,1,3,6,10,12,14)$



With AND2 gates



(6 AND gates)

1 AND-2 gate ≡ 2 NAND-2 gates

6 AND-2 gates ≡ 12 NAND-2 gates

12 NAND-2 gates (for AND-7) + 7 NAND-2 gates (for inverters) = **19 gates**