

EHB322E Digital Electronic Circuits

QUIZ I

Duration: 60 Minutes

Grading: 1) 50%, 2) 50%

For your answers please use the space provided in the exam sheet

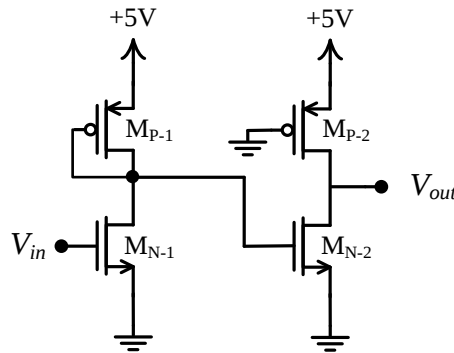
GOOD LUCK!

- 1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} [2(V_{GS} - V_{T0p,n})V_{DS} - V_{DS}^2]$

Transistor parameters: $k_p' = \mu_p C_{ox} = 35 \mu A/V^2$, $k_n' = \mu_n C_{ox} = 98 \mu A/V^2$, $V_{TN} = 1V$, $V_{TP} = -0.5V$, $W_{N-1} = 5\mu$, $W_{N-2} = 5\mu$, $L_P = L_N = 1\mu$.



Buffer

- Find the maximum value of W_{P-1} satisfying that $V_{in} = 5V$ results in $V_{out} = 5V$.
- Find the value of W_{P-2} if $V_{in} = 0V$ results in $V_{out} = 1V$.
- Find the buffer's static power consumption values when $V_{in} = 0V$ and $V_{in} = 5V$.

a) $V_{out} = 1V \Rightarrow \frac{1}{2} \cdot 98 \mu \frac{5}{1} \{2(4) \cdot 1 - 1^2\} = \frac{1}{2} \cdot 35 \mu \frac{W_{P-1}}{1} \{(4 - 0.5)^2\}$ (20)

$\Rightarrow W_{P-1} = 8 \mu$

b) $V_{out} = 4.5V \Rightarrow \frac{1}{2} \cdot 98 \mu \cdot 5 \{2(2.5) \cdot 1 - 1\} = \frac{1}{2} \cdot 35 \mu \frac{W_{P-2}}{1} \{2(4.5) \cdot 4 - 4^2\}$ (20)

$\Rightarrow W_{P-2} = 4.2 \mu$

c) $V_{in} = 0V \Rightarrow I_{total} = I_{DN-2} = 1.47 mA$ $P = 5 \cdot 1.47 = 7.35 mW$

$V_{in} = 5V \Rightarrow I_{total} = I_{DN-1} = 1.715 mA$ $P = 5 \cdot 1.715 = 8.6 mW$ (10)

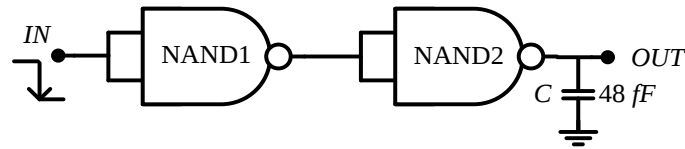
- 2) Consider a buffer circuit consisting of two CMOS NAND gates, shown below. An external capacitor of 48fF is connected to the output. A signal switching from high to low is applied to the input.

Equivalent resistor for an NMOS transistor: $R_N = (12\text{k}\Omega) / (W/L)_N$

Equivalent resistor for a PMOS transistor: $R_P = (24\text{k}\Omega) / (W/L)_P$

Gate capacitors $C_{GS-N} = c_{ox}W_NL_N$ and $C_{GS-P} = c_{ox}W_PL_P$; neglect C_{GD} capacitors.

Transistor parameters: $c_{ox} = 1\text{ fF}/\mu\text{m}^2$, $L_N = L_P = 1\mu$, $W_{N1} = 2\mu$, $W_{P1} = 3\mu$, $W_{N2} = 4\mu$, $W_{P2} = 6\mu$.



Digital circuit with two CMOS NAND gates

- Implement a NAND gate with a Boolean function $f = \overline{x_1x_2}$ using CMOS transistors. If inputs of a NAND gate are shorted, as we use in our circuit, then find its Boolean function. Draw the CMOS implementation of the above circuit.
- Find the **total propagation delay value** (delay of NAND1 + delay of NAND2) between the input and the output.
 - You should consider C_{GS} capacitors as well as the external $C = 48\text{fF}$ capacitor
 - Do not consider capacitors at nodes other than the node of gate inputs/outputs.

a)

$f = x_1x_2$

If $x_1 = x_2$
 $f = \overline{x_1} \rightarrow \text{inverter}$

b)

Output of NAND1 $\Rightarrow C_1 = (4 \times 6) \times 1\text{ fF} = 24\text{ fF}$

Output of NAND2 $\Rightarrow C_2 = C = 48\text{ fF}$

$R_{N-1} = 6\text{ k}\Omega$	$R_{N-2} = 3\text{ k}\Omega$
$R_{P-1} = 8\text{ k}\Omega$	$R_{P-2} = 4\text{ k}\Omega$

total delay = $t_{PLH-1} + t_{PLH-2}$

$$= 0.69 \left((R_{P1} // R_{N1}) \cdot C_1 \right) + 0.69 \left((R_{N2} + R_{N-1}) C_2 \right)$$

$$= 0.69 (4\text{ k}\Omega \cdot 24\text{ fF} + 6\text{ k}\Omega \cdot 48\text{ fF}) \approx 0.251\text{ ns}$$

20 254 ps //