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Student ID:

EHB322E Digital Electronic Circuits
Homework 2

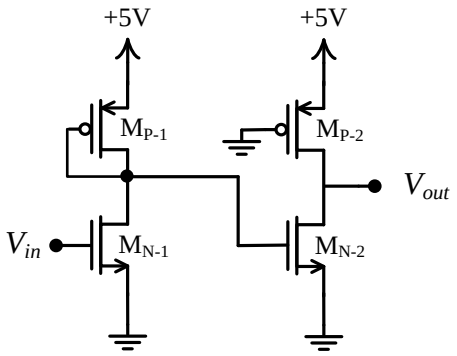
Grading: 1) 30%, 2) 30%, 3) 40%
Deadline:20/04/2020 (before 16:30)
Email your homeworks to the teaching assistant or submit via Ninova

1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0\,p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} \left[2(V_{GS} - V_{T0\,p,n})V_{DS} - V_{DS}^2\right]$

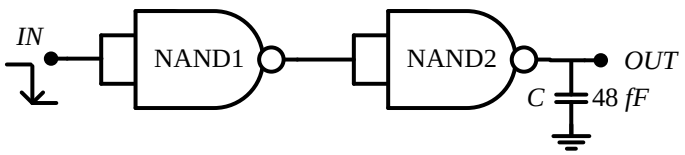
Transistor parameters: $k_p' = \mu_p c_{ox} = 35\text{uA/V}^2$, $k_n' = \mu_n c_{ox} = 98\text{uA/V}^2$, $V_{TN}=1\text{V}$, $V_{TP}=-0.5\text{V}$, $W_{N-1}=5\text{u}$, $W_{N-2}=5\text{u}$, $L_P=L_N=1\text{u}$.



Buffer

a) Find the maximum value of $\mathbf{W_{P-1}}$ satisfying that $\boldsymbol{V_{in}}$**=5V** results in $\boldsymbol{V_{out}}$**= 5V**.
b) Find the value of $\mathbf{W_{P-2}}$ if $\boldsymbol{V_{in}}$**=0V** results in $\boldsymbol{V_{out}}$**= 1V**.
c) Find the buffer's static power consumption values when $\boldsymbol{V_{in}}$**=0V** and $\boldsymbol{V_{in}}$**=5V.**

2) Consider a buffer circuit consisting of two CMOS NAND gates, shown below. An external capacitor of 48*fF* is connected to the output. A signal switching from high to low is applied to the input.
Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= (12kΩ) / (W/L)$_N$**
Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= (24kΩ) / (W/L)$_P$**
Gate capacitors $\boldsymbol{C_{GS-N}} = c_{ox} W_N L_N$ and $\boldsymbol{C_{GS-P}} = c_{ox} W_P L_P$; neglect $\boldsymbol{C_{GD}}$ capacitors.
Transistor parameters: $c_{ox}=1$ fF/um2, $L_N=L_P=1\text{u}$, $W_{N1}=2\text{u}$, $W_{P1}=3\text{u}$, $W_{N2}=4\text{u}$, $W_{P2}=6\text{u}$.



Digital circuit with two CMOS NAND gates

a) Implement a NAND gate with a Boolean function $f = \overline{x_1 x_2}$ using CMOS transistors. If inputs of a NAND gate are shorted, as we use in our circuit, then find its Boolean function. Draw the CMOS implementation of the above circuit.

b) Find the **total propagation delay value** between the input and the output.

- You should consider C_{GS} capacitors as well as the external C=48fF capacitor
- Do not consider capacitors at nodes other than the node of gate inputs/outputs.

3) For a specific technology and a specific supply voltage, a CMOS inverter with parameters W_P=1u, W_N=1u, L_P=1u, L_N=1u, and a total output load capacitor of 1 fF has t_{PHL} =1ns and t_{PLH} =2ns. By considering the same technology and the supply voltage,

a) Implement $f = x_1 x_2 \overline{x_3} + x_1 \overline{x_2} x_3 + \overline{x_1} x_2 x_3 + \overline{x_1} x_4$ with a **CMOS circuit** using **minimum** number of transistors. Draw the circuit. How many PMOS and NMOS transistors do you use?

b) Select W_P=4u for all PMOS transistors and W_N=2u for all NMOS transistors of your CMOS circuit. Find the **worst case (largest) and** the **best case (smallest)** $\boldsymbol{t_{PHL}}$ and $\boldsymbol{t_{PLH}}$ values if a total output load capacitor is 2 fF. Neglect internal node capacitors. You should report 4 delay values.