Student Name: **Instructor: Mustafa Altun**

Student ID:

Date & Time: 02/07/2020 & 12:00

EHB322E Digital Electronic Circuits
Final Exam

Duration: 150 Minutes
Grading: Q1) 20%, Q2) 20%, Q3) 20%, Q4) 20%, Q5) 20%
Exam is open-source
GOOD LUCK!

Q1

a) What are the advantages of digital circuits compared to analog ones?

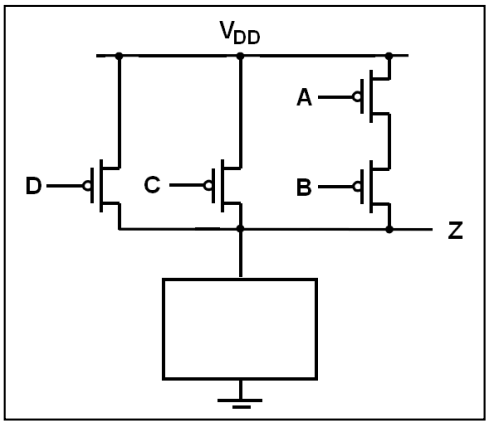
b) What are the advantages of dynamic digital circuits compared to static ones?

c) How does wiring affect delay and digital signals?

d) Which paramaters affect digital power consumption?

Q2

a) For the CMOS complex gate in the figure, find the logic function Z and draw the pull-down circuit in the box.



b) Suppose that minimum W/L's for both NMOS and PMOS transistors are 1 that results in ReqN and ReqP equivalent resistors in a CMOS inverter. If W/L's are selected as 2 in our circuit, determine the worst case equivalent pull-up and pull-down resistors in terms of ReqN and ReqP.

c) Which input combination with transitions give the worst case delays? Consider all node capacitors.

Q3

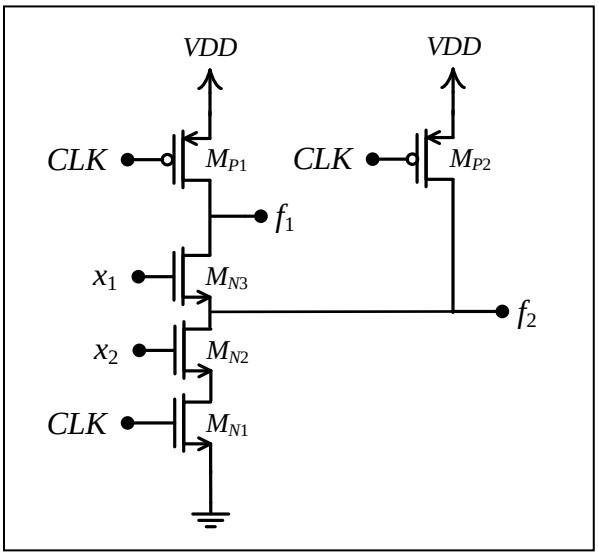
Implement $Y = \overline{X1}.X2 + X1.\overline{X3}$ with Pass Transistor Logic by using only NMOS transistors with an order of X1-X2-X3..

a) Draw the circuit.
b) Suppose that the output capacitor of the circuit is C_L=0.1pF. Neglect other node capacitors. Also the equivalent resistor for an NMOS transistor is R_{eq}=10kΩ. Find the propagation delay if the inputs change from X1=0, X2=1, X3=1 to X1=0, X2=0, X3=0.

Q4

Consider the CMOS dynamic circuit shown in the figure.

a) Derive expressions of f_1 and f_2 in terms of the inputs when ***CLK***=0.
b) Derive expressions of f_1 and f_2 in terms of the inputs when ***CLK***=1.
c) For f_1 calculate the **worst case** t_{PHL}. Each node has an equivalent capacitor of **0.1pf** and each transistor has an equivalent resistor of **1kΩ.** Suppose that all input transitions happen in pre-charge phase and each circuit node has an initial voltage value of either GND or VDD.



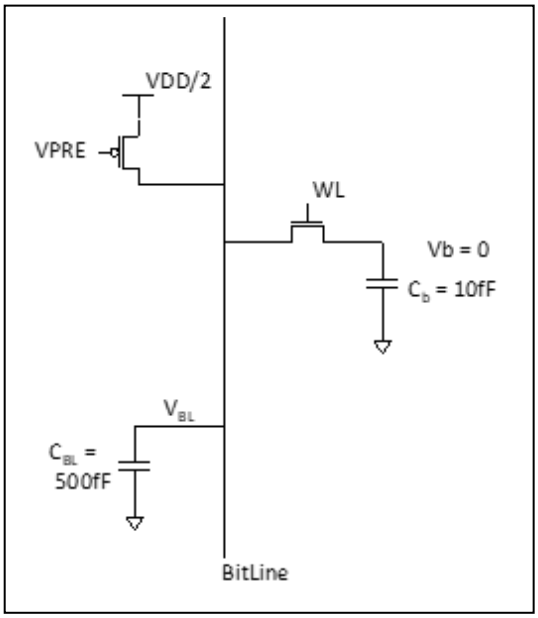
Q5

For the DRAM cell.VDD=3.3V Assume NMOS and PMOS transistors are ideal switches. ($R_{sw(on)}$=0)

The bitline is precharged to VDD/2 when VPRE=0 and WL=0.

The bit that needs to be read is 0 (Vb = 0V) when VPRE = 1 and WL = 1.

What is the voltage at bitline V_{BL}=? That needs to be detected.



$$T_{PHL} \cong \frac{C_L}{\beta_N}\frac{1}{2} \qquad T_{PLH} \cong \frac{C_L}{\beta_P}\frac{1}{2} \qquad t_P \cong 0{,}7xRC$$

$$V_{th} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{\beta_N}{\beta_P}}V_{TN}}{1+\sqrt{\frac{\beta_N}{\beta_P}}} \qquad \frac{W_N}{W_P} \cong \frac{1}{2}\frac{\mu_p}{\mu_n}\frac{(V_{DD}-V_T)}{V_{OL}}$$

(Saturation) $I_D = \frac{1}{2}\beta(V_{GS}-V_T)^2$ (Linear) $I_D = \beta(V_{GS}-V_T-\frac{V_{DS}}{2})V_{DS}$