25.05.2016

**DIGITAL ELECTRONIC CIRCUITS**

**Final Exam**

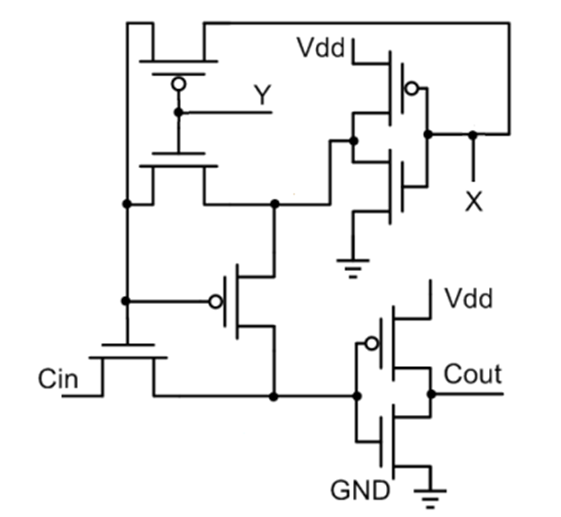
Closed notes and books.

Duration: 120 minutes.

**1.** For a CMOS process, VDD= 5 V, μnCox=60 μA/V2, μpCox=20 μA/V2, VTN=0.6 V, VTP= -0.6 V, Lmin= 0.35 μm are given.

1. Sketch the standard CMOS circuit which realizes the function Z=(AB+C)’+(D+E+F)’.
2. Calculate WP /WN ratio for all transistors so that τPLH /τPHL=3 for the worst case conditions (MN=MP=M since VTN= -VTP ).
3. Using the ratio found in b), find the switching threshold VTH if all inputs switch simultaneously.
4. Sketch the circuit that realizes the same function using pseudo-NMOS logic. Calculate VOL by using the ratio found in b). Justify the results.

**2.** Consider a circuit shown below. Suppose that all NMOS transistors are identical and all PMOS transistors are identical. *Equivalent resistor for an NMOS transistor:* ***RN=*4kΩ**. *Equivalent resistor for a PMOS transistor:* ***RP=*12kΩ**. Suppose that each circuit node (including outputs) has a capacitance value of **1pF**.

1. Derive a Boolean expression for the output **Cout** in terms of the inputs **X**, **Y**, and **Cin.**
2. If **X=1→0**, **Y=1**, and **Cin=1**, calculate the propagation delay (**tPLH**  or **tPHL**) at the output.

**3.**

1. Implement logic functions Y=[ABC+D(E+F)]’ and Z=G’Y’ using a dynamic 2-level circuits.
2. Implement the functions in a) using domino logic and sketch them.
3. For input assignments of ABCDEFG=1111111, explain how the implemented circuit in a) works when CLK=0 and CLK=1.

**4.**

2-to-4 LINE DECODER

NMOS

NAND

MEMORY

Y0

Y1

Y2

Y3

W2

W3

W1

W0

A1

A0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A0 | A1 | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |

Suppose that the above structure is a pseudo-NMOS NAND type read-only-memory (ROM) with 4 word-lines W0-W3 and 4 bit-lines Y0-Y3. Sketch circuit implementations of the decoder and the memory.

**5.** Answer the following questions shortly.

1. Explain the storage capacity of dynamic memories.
2. State the differences between EPROM and E2PROM.
3. State the differences between RAM and E2PROM.
4. State the problem if an NMOS pass transistor logic circuit drives a static CMOS circuit/gate.
5. Why is the supply voltage decreased with the emerge of new technologies?





