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EHB322E Digital Electronic Circuits
MIDTERM II

Duration: 120 Minutes

Grading: 1) 60%, 2) 40%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

GOOD LUCK!

g = $x_4 x_5$

1) Consider a Boolean function $f = g x_2 x_3 + \overline{x_1}\,\overline{x_2} + x_1\,\overline{x_3}$ where $g = x_4 + x_5$.
Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
V_{DD}=5V and $|V_{TH}| = 1V$ (Both for NMOS and PMOS).
Equivalent resistor for an NMOS transistor: R_N= **12kΩ**
Equivalent resistor for a PMOS transistor: R_P= **24kΩ**
Suppose that the output circuit node has a capacitance value of **10pF**. Neglect internal and other node capacitors.

6t
12t

Implement ***f*** with "NMOS Pass Transistor Logic – PTL - Network(s)" and "CMOS Inverters" with minimum number of transistors such that there is no threshold voltage drop at the output (output is VDD or GND all the time). For the PTL networks use the ordering of $x_1 - x_2 - x_3 - x_4 - x_5$. Also use only variables $x_1 - x_2 - x_3 - x_4 - x_5$ as inputs, not their negated forms. Find the **minimum number** of transistors needed. Find the **worst case (largest)** t_{PHL} **and** t_{PLH} values (total of 2 values).

$g = x_4(1) + \overline{x_4}(x_5)$ $\quad g = x_4(x_5) + \overline{x_4}(0)$

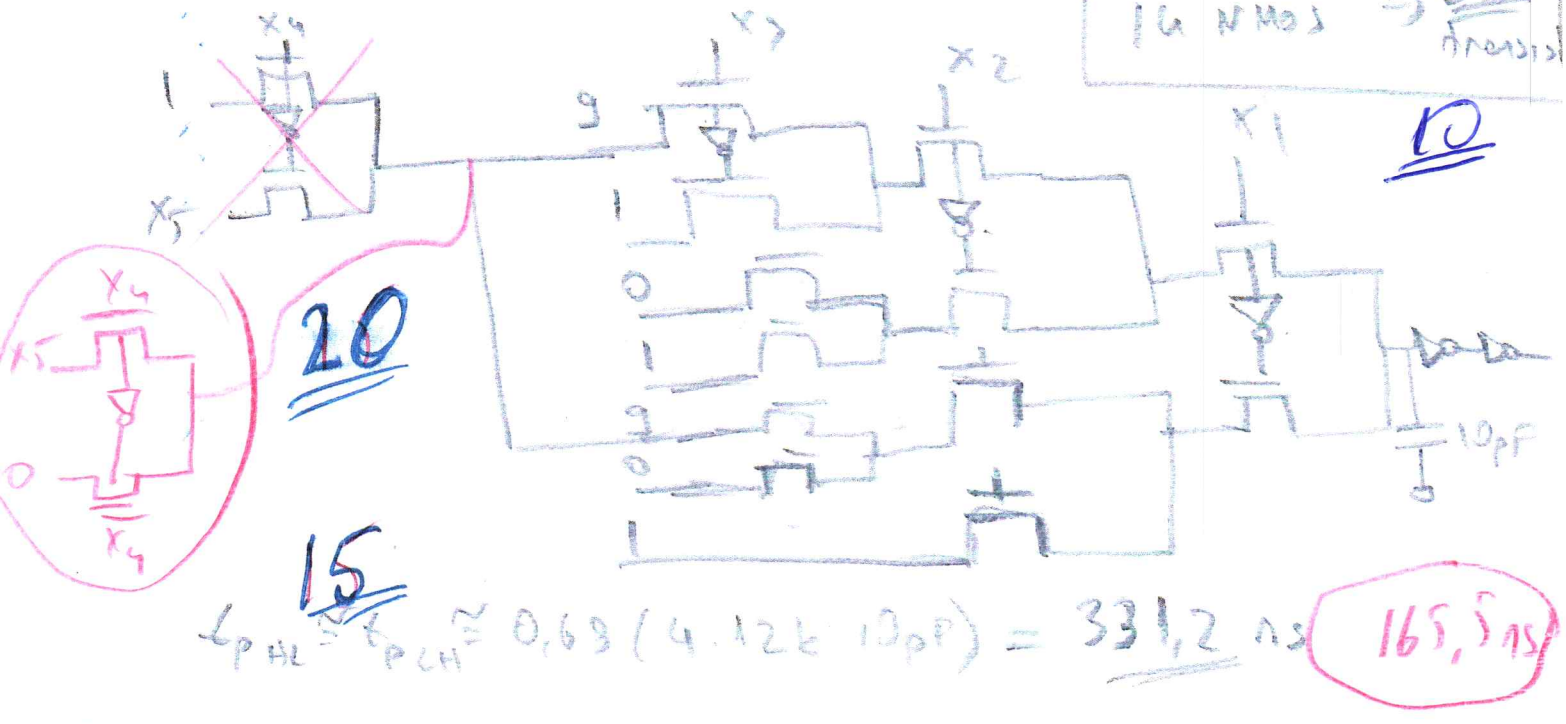
$f = x_1(x_2 x_3 g + \overline{x_3}) + \overline{x_1}(x_2 x_3 g + \overline{x_2}) = x_1\left(x_2(x_3 g + \overline{x_3}) + \overline{x_2}(\overline{x_3})\right) +$

15 $= x_1\left(x_2(x_3(g) + \overline{x_3}(1)) + \overline{x_2}(x_3(0) + \overline{x_3}(1))\right) \quad \overline{x_1}\left(x_2(x_3 g) + \overline{x_2}(1)\right)$

$+ \overline{x_1}\left(x_2(x_3(g) + \overline{x_3}(0)) + \overline{x_2}(1)\right)$

6 inverter
16 NMOS $\Rightarrow$ 26 transistor

10



20

15

$t_{PHL} \cong t_{PLH} \cong 0{,}69(4.12k \cdot 10pF) = 331{,}2\ ns$

165,5 ns

g= $x_4 x_5$

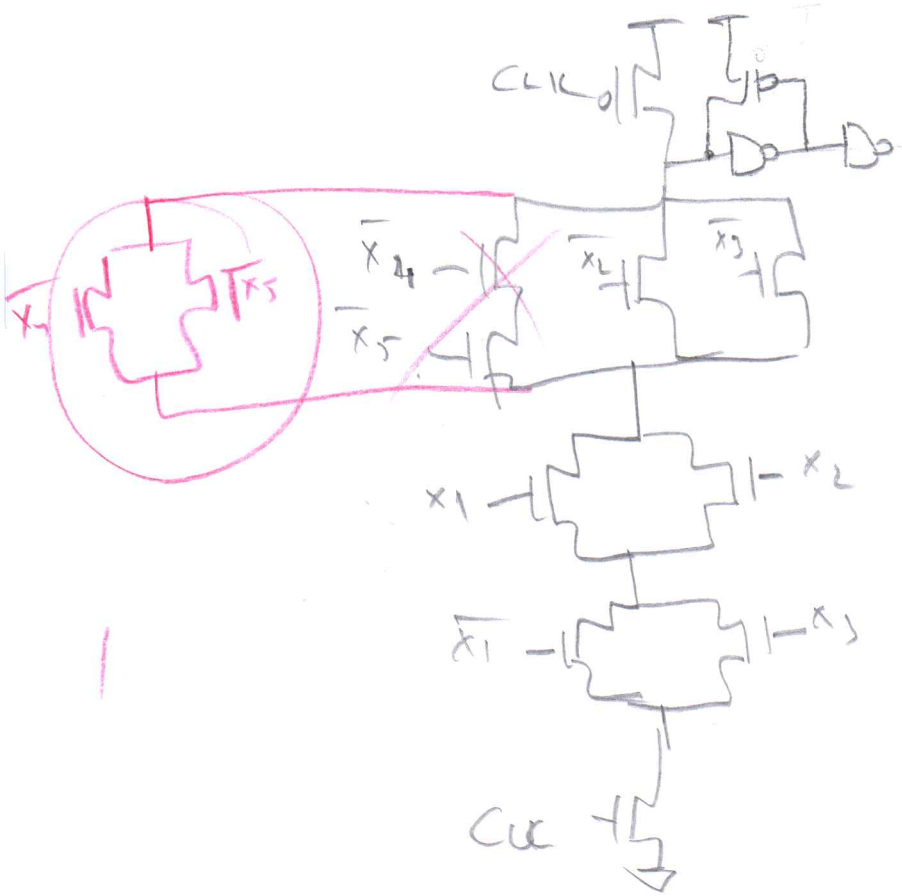
2) Consider a Boolean function $f = g x_2 x_3 + \overline{x_1}\,\overline{x_2} + x_1\,\overline{x_3}$ where $g = x_4 + x_5$. Implement ***f*** with "Dynamic Logic" using "a Pull-Down NMOS Network" using minimum number of transistors such that there is no charge sharing problem. Find the **minimum number** of transistors needed.

Equivalent resistor for an NMOS transistor: R_N**=12kΩ**

Equivalent resistor for a PMOS transistor: R_P**=24kΩ**

Suppose that the output circuit node has a capacitance value of **10pF**. Neglect internal and other node capacitors. You can use variables $x_1 - x_2 - x_3 - x_4 - x_5$ and their negations as inputs. Find the **worst case (largest)** t_{PHL} **and** t_{PLH} values (total of 2 values).

$f = x_2 x_3 (x_4 + x_5) + \overline{x_1}\,\overline{x_2} + x_1 \overline{x_3}$



10pF 20

10 transistors + 5 transistors

wc $t_{PHL} = 0{,}69\ 5(12k)\ 10p = 414ns$ 10

wc $t_{PLH} = 0{,}69\ 24k\ 10p = 165{,}6ns$ 10

wc $t_{PHL} = 0{,}69\ (4 \times 6k)\ 10p = 165{,}6ns$

wc $t_{PLH} = 0{,}69\ 12k\ 10p = 82.8ns$