Skybridge 3D Connect for Surface Computing

1. Introduction

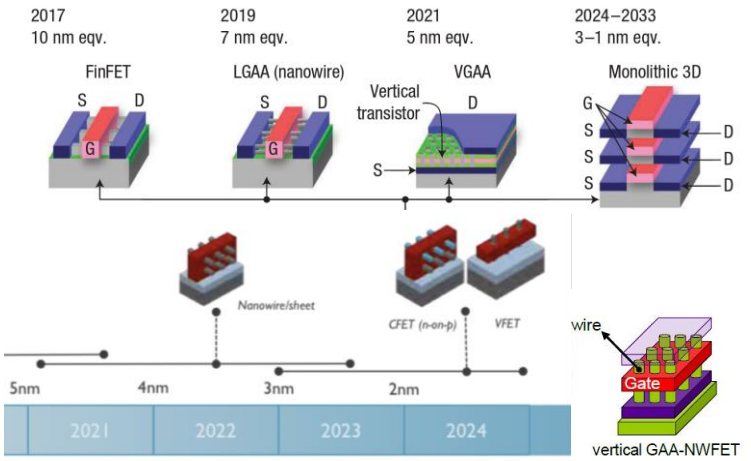

Figure 1. A) IRDS projecting need for a Vertical 3D monolithic approach from 2024 on [18]; B) IMEC's roadmap towards Vertical Nanowire FET (VFET, GAAs) based CMOS from 2024 on [19].

This work extends the NSF grant no. 1407906 (PI: Moritz) toward exploring a fabric that provides 3D connectivity required for implementing dense circuit architectures that require high degree of connectivity. Examples include Artificial Neural Networks (ANNs) requiring crossbar array-based computing with nanoscale devices as well as crossbars that implements mathematical functions efficiently. Crossbar arrays consisting of nanoscale devices have received significant interest in the computing community lately. Ease of manufacturability of large, dense arrays with emerging nanoscale devices e.g., four-terminal switches, memristors, phase-change devices etc., located at each crosspoint has paved way for a wide variety of applications ranging from Boolean function implementation[1] to neuromorphic computing[2][3][4]. However, if crossbar arrays are used to implement circuit architectures with large connectivity, wiring the devices to selectively control each device becomes intractable as the size of the array increases. To illustrate the problem further, consider the case of four-terminal switch-based arrays used for implementing Boolean logic functions and memory elements. Any arbitrary Boolean function can be implemented by selectively turning on/off the switches arranged in a regular 2D lattice[1]. If routing of the switch control signals were to follow the conventional CMOS's two-dimensional routing mindset, it would lead to severe pin and routing congestion ultimately leading to interconnect bottleneck in large lattices thus diminishing the benefits of this approach and limiting scalability. Hence the biggest challenge in implementing ANNs and other computational models is often supporting the high degree of connectivity required for wiring the nanoscale devices in the crossbar arrays.

3D-based fabric directions are critical in surpassing many of the current limitations in traditional CMOS scaling, including interconnection bottlenecks[5][6][7][8][9][10][11][12]. A direction the research community previously explored is based on stacking layers of conventional 2D CMOS and connecting these layers with inter-layer vias. The technologies following this mindset are collectively called as Monolithic 3D technology (M3D). The key idea of this appraoch is the 3D sequential integration of tiers thus not requiring precision alignment of tiers like in TSV 3D integration[5]. If this technology were to be used for implementing crossbar array-based circuits, the nanoscale devices would be fabricated in the bottom tier whereas routing of the switch control signals would be carried out on the top tier. However, it would still lead to severe pin/routing issues because it follows the conventional 2D CMOS routing on the top tier.

One of the prominent works in the direction of mitigating the issues of various 3D directions is SkyBridge-3D-CMOS (S3DC). S3DC is a fine-grained 3D fabric which envisions a *systematic way of building static CMOS circuits in a skeleton-style vertical nanowire structure*. To form the pull-up and pull-down networks containing series / parallel connections, series networks are built with active devices on one nanowire, and parallel networks are built by placing and connecting devices across nanowires. Several innovative fabric

structures enable static CMOS gates in 3D with a primarily material deposition assembly and single-wafer processing[13][14][15][16][17]. S3DC 3D integration is vertical, featuring unique connectivity approaches, allowing flexibility in all three dimensions making it suitable for high connectivity architectures such as ANNs. *These directions align perfectly with both IMEC and IRDS (formerly ITRS) roadmaps* (see Figs. 1A, 1B), projecting that a vertically-integrated direction, including with fine-grained vertical GAAs on nanowires, is a key path beyond 2024.

Leveraging the aspects of SkyBridge-3D-CMOS for 3D routing and transistor-level Monolithic-3D technology's tier-by-tier processing, we propose SkyBridge-3D-Connect(S3C). S3C is a 3D fabric architected for wiring/routing highly dense circuits such as crossbar-based arrays like in four-terminal lattices and potentially other emerging device-based arrays typically used for ANNs, Bayesian Networks etc. S3C follows the tier-by-tier processing technique as in M3D with Monolithic Interlayer Vias (MIV) used for connectivity between the tiers. The bottom tier would contain the nanoscale devices fabricated in a crossbar array whereas the top tier would contain the MIVs and silicon nanowires along with the 3D routing features such as in S3DC. The control-gate terminals are connected to the top-tier using MIVs. The signals from the MIVs are routed using S3DC style 3D routing features thus providing a high degree of connectivity essential for implementing the crossbar array circuits.

2. Background Work: SkyBridge-3D-CMOS (S3DC)

This is the first fine-grained 3D CMOS IC technology fully leveraging the vertical dimension. It also tackles the routing challenges with its novel fabric-level concepts. First, all circuits are realized on a uniform vertical silicon nanowire template – shown in Fig. 2A-B. We place and connect active devices on these nanowires either in series (on one nanowire) or in parallel (across multiple nanowires connected in parallel) to build CMOS circuits. Template nanowires are pre-doped (doping happens at wafer-level) enabling n- and p-type JL nanowire device formation with material deposition. *The p- and n-layering is achieved with initial wafer bonding of a p- and an n- type wafers before any other step*; each wafer is doped similar to [6]. This is a *simpler process vs. M3D's wafer formation that requires bonding after the bottom layer circuits are fully completed*. Nanowires are formed through etching. Parallel networks are built with devices on different vertical nanowires; these are shorted together on both drain and source sides. S-ILC is the specially-designed structure that connects the p-type pull-up and n-type pull-down networks together to generate the output signal. We also wire several S-ILCs together to short the nanowires and form a parallel network. The S-ILC structure is shown in Fig. 2C. It is designed to provide connection between the two layers with small parasitic resistance and capacitance. Materials are chosen based on the favored work function: e.g., Ni and Ti are chosen to form good Ohmic contacts with p- and n-doped silicon nanowires,

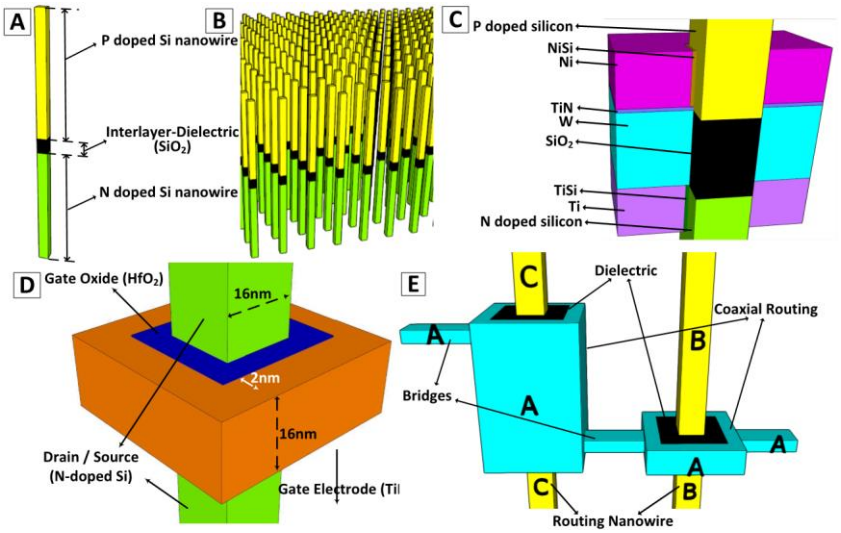

Figure 2. Fabric components: A) One single nanowire with striped doping; B) Uniform vertical nanowire template; C) An n-type V-GAA JL transistor in 16nm S3DC technology; D) S-ILC allows routing between various doping layers without MIVs; E) 3D connections within one doping layer realized by Bridges, Coaxial Routings, and routing nanowires; three signals A, B, C are carried in this example.

respectively. S3DC fabric components have been validated using TCAD simulations with nanoscale effects taken into consideration.

Other S3DC fabric components include:

- Routing Nanowires are vertical nanowires (See Fig. 2E). They are silicided, having high conductivity.
- Routing Bridges (See Fig. 2E) are horizontal metal wires connecting adjacent nanowires.
- Uniform Vertical Gate-All-Around (V-GAA) JL transistors. An n-type transistor structure is shown in Fig. 2D. The source, channel, and drain regions are based on heavily doped vertical nanowires. Carefully selected gate electrodes and dielectric materials are surrounding the nanowire. The V-GAA behavior is modulated by the work function difference between gate and channels[20].
- Coaxial Routing structures (See Fig. 2E) are metal layers formed along the vertical routing nanowires (with insulating oxide ring) to add connectivity in vertically. We optimized the material types and geometry so that these metal layers have negligible influence on the functionality of the nanowires.

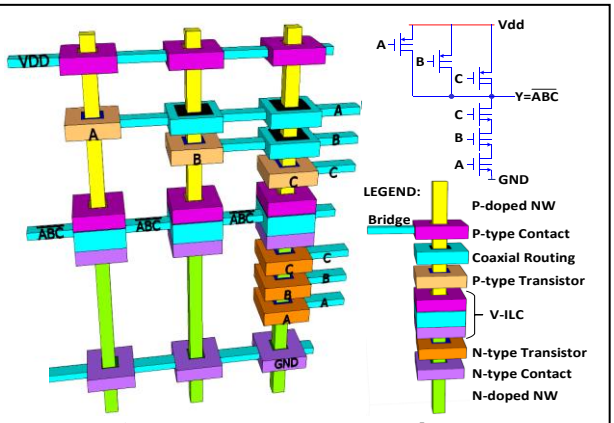

Figure 3. S3DC 3-in NAND layout

For additional intuition please see Fig. 3. It shows a three-input S3DC NAND gate as an example of a logic-implementing static CMOS circuit utilizing the above concepts. The three p-type transistors on the top are connected at the source side by VDD, and on the drain side by the V-ILCs. Thus, the pull-up network is parallel. Three n-type transistors at the bottom are connected in series by the vertical nanowire. They form the pull-down network. S-ILCs connect the pull-up and pull-down networks to generate the output signal, which is conducted out by the Bridges. VDD and GND are delivered to each cell through the Bridges in the top and the bottom layer. These two layers are reserved only for power delivery, which ensures enough resources to deliver power with minimal IR drop. In S3DC technology, transistor sizing can be achieved by connecting multiple transistors in parallel across neighboring nanowires. This transistor sizing method is like FinFETs and is quantized. The *pin access* to S3DC cells is greatly improved using the vertical dimension better. Table I provides a comparison between key aspects of S3DC and other 3D directions. In the proposal we focus on a 16-nm S3DC technology-node, but a possible roadmap will be explored.

Table I. TSV-3D, M3Ds, vs. S3DC

	TSV-3D	**TR-L/G-L M3D**	**S3DC**
Routing Elements	Uses conventional 2D routing elements, added connectivity from TSVs	Uses conventional 2D routing elements, connectivity w. MIVs	Full 3D (vertical nanowire; Coaxial Routing; Bridges within one active layer, V-ILC between layers).
Pin Access	Pin access limited by cell surface	Decreased pin access, limited by horizontal cell surface	Improved pin access from its 3D routing scheme.
Granularity	Coarse-grained (limited by TSV alignment [5])	Finer-grained (Cell- or transistor-level [21], layer-by-layer)	Vertically-composed fine-grained in S3DC
Process	Separate process for each layer	Sequential layer-by-layer. Wafer bonding with first layer finished.	Processed as a single wafer in V3DC

3. Proposed Work: SkyBridge-3D-Connect (S3C) Fabric

3.1. S3C Fabric Design

We propose to explore Skybridge-3D-Connect(S3C) fabric. S3C combines the innovative routing of S3DC with M3D's tier-by-tier assembly to implement a 3D fabric technology suitable for implementing architectures which require high degree of connectivity such as ANNs as well as four-terminal lattice-based computing. Fig. 4 shows implementation of 2x2 switch lattice in S3C fabric. S3C follows the M3D's

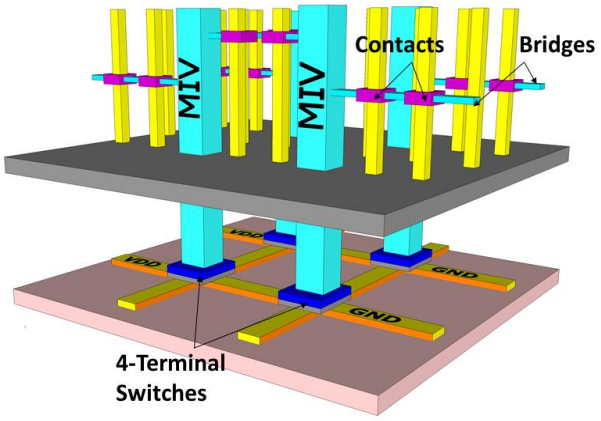

Figure 4. 2x2 switch lattice in S3C fabric. Shows S3C fabric architecture consisting of two molecular bonded wafers and vertical routing elements.

sequential stacking assembly with tier-by-tier processing. The assembly begins with the processing of the bottom tier.

First, 2D crossbar devices are fabricated in the bottom semiconductor wafer tier using material deposition techniques such as e-beam evaporation. In case of the four-terminal switch lattice, the vertical nanodevice stack consists of doped horizontally crossed nanowires followed by an insulator and then followed with a metal gate. After this, a thin layer of dielectric is deposited and planarized on top of the nanodevices.

This is followed by a low temperature molecular bonding of the wafers wherein the top tier will implement routing features as well as create MIVs that will go all the way through both tiers. The top tier implements the S3DC features such as doped silicon nanowires through RIE etching, co-axial routing structures and horizontal metal bridges through selective material deposition. The interlayer dielectric is etched to expose the metal gates of the nanodevices. MIVs are metal vias that are deposited in the etched areas to provide connectivity between the two substrates. The MIVs are connected to nanowires through Skybridge metal bridges connected at different levels thus improving the pin access – these features are already demonstrated experimentally in our group. These 3D routing features allow for connectivity in three dimensions mitigating the routing congestion problems in dense 2D circuit architectures requiring high connectivity.

3.2. S3C Device-to-System Design and Evaluation Tasks

We will explore various aspects of this fabric including its material structure and design, as well as manufacturability related processes. We will also investigate CAD tool support such as synthesis, technology mapping, physical design for the S3C fabric.

The various S3C routing features will be characterized using detailed physics-based 3D simulation of the electrostatics and operations using Synopsys Sentaurus TCAD[22]. The Sentaurus Process can be used to create the structures emulating an actual process flow.

We will collaboratively project the benefits of using routability of the S3C fabric for various applications such as four-terminal lattice-based computing, ANNs etc.

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