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Student ID:

EHB205E Introduction to Logic Design
Homework 2

Deadline: 19/11/2021 (before 9:30)

PART 1

1) Get Xilinx ISE 14.7 webpack from https://www.xilinx.com/support/download.html. Install to your computer.
2) Take "OR_gate.vhd" and "OR_gate_tb.vhd" files from ninova.
3) Start "Project Navigator" in "ISE Design Tools" in Xilinx ISE.
4) Build a new project by "New Project" command. Give a name to your project.
5) Add the files mentioned above by "Add Source" command in "Project" tab.
6) When the option is "view" "implementation" and "OR_gate.vhd" is chosen, view your circuits schematic by "view RTL schematic" in "Synthesize" list. Take the picture in order to use in your homework report.
7) Choose "view" "Simulation" option.
8) When "OR_gate_tb.vhd" file is chosen, push "Simulate Behavioral Model" command. You should see a graph with inputs and outputs. Take a picture of this graph between 0 ns – 60 ns for your homework report.
9) Prepare a report which shows that you succesfully completed all the above steps.

PART2

10) Create a new project as explained in the first part.
11) Take "OR_gate.vhd" and "OR_gate_tb.vhd" files from here or from Ninova. You will design your circuit by changing these files.
12) "Save As" "OR_gate.vhd" file by giving name "Boolean_Function_Case_Statement.vhd" that will be used to define one of your designs.
13) Add your "Boolean_Function_Case_Statement.vhd" file by "Add Sources", "Add or create design sources" to your project.
14) Change the names and the number of inputs and outputs according to the truth table given below. You have four inputs, a_1, a_0, b_1, b_0 and three outputs, c_2, c_1 and c_0.

a_1	a_0	b_1	b_0	c_2	c_1	c_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

15) Change the data types of inputs and outputs according to the examples given in the following web pages

- http://www.csit-sun.pub.ro/courses/Masterat/Materiale_Suplimentare/Xilinx%20Synthesis%20Technology/toolbox.xilinx.com/docsan/xilinx4/data/docs/xst/vhdl3.html
- https://startingelectronics.org/software/VHDL-CPLD-course/tut13-VHDL-data-types-and-operators/
- http://www.brunel.ac.uk/~eestmba/hdl/dtypevhdl1.html
- https://en.wikibooks.org/wiki/Programmable_Logic/VHDL_Data_Types
- https://web.engr.oregonstate.edu/~sllu/vhdl/lec2e.html

16) Describe the functionality of your circuit under "architecture begin" by using "case statement" as given in the following web pages

- https://www.ics.uci.edu/~jmoorkan/vhdlref/cases.html
- https://www.nandland.com/vhdl/examples/example-case-statement.html
- https://www.allaboutcircuits.com/technical-articles/sequential-vhdl-if-and-case-statements/
- http://vhdl.renerta.com/mobile/source/vhd00014.htm
- https://insights.sigasi.com/tech/signal-assignments-vhdl-withselect-whenelse-and-case/

17) Make sure that "Boolean_Function_Case_Statement.vhd" is your top module. You can change top module by right click to the module that you would like to implement and choose "Set as Top" from the list. Produce the RTL schematic of your design.

18) "Save As" "OR_gate_tb.vhd" file by giving name "Boolean_Function_Case_Statement_tb.vhd" that will be used to describe your testbench for simulation of your design.

19) Add your "Boolean_Function_Case_Statement_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.

20) Write the test bench file to test your design by using "Boolean_Function_Case_Statement_tb.vhd". You can find examples to write testbenches in VHDL in the following web pages. Simulate your design, produce wave form for your report.

- https://vhdlguide.readthedocs.io/en/latest/vhdl/testbench.html
- https://www.fpgatutorial.com/how-to-write-a-basic-testbench-using-vhdl/
- https://allaboutfpga.com/vhdl-testbench-tutorial/
- https://technobyte.org/testbench-vhdl-types-examples-steps/

21) "Save As" "Boolean_Function_Case_Statement.vhd" file by giving name "Boolean_Function_Data_Flow.vhd" that will be used to describe your second design.

22) Add your "Boolean_Function_Data_Flow.vhd" file by "Add Sources", "Add or create design sources" to your project.

23) Add your "Boolean_Function_Data_Flow.vhd" file to your project.

24) Describe the functionality of your circuit under "architecture begin" by using "data flow modelling" as given in the following web pages

- https://vhdlguide.readthedocs.io/en/latest/vhdl/dataflow.html
- https://www.oreilly.com/library/view/vhdl/9788131732113/xhtml/chapter005.xhtml
- https://buzztech.in/vhdl-modelling-styles-behavioral-dataflow-structural/
- https://www.technobyte.org/vhdl-code-for-an-encoder-dataflow/

25) Make sure that your "Boolean_Function_Data_Flow.vhd" is your top module. Produce the RTL schematic of your design.

26) "Save As" "Boolean_Function_Case_Statement_tb.vhd" file by giving name "Boolean_Function_Data_Flow_tb.vhd" that will represent your testbench for simulation of your second design represented in Part 2.15.

27) Add your "Boolean_Function_Data_Flow_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.

28) Write the test bench file to test your design by using "Boolean_Function_Data_Flow_tb.vhd". Simulate your design.

References

1) Morris Mano, Micheal Ciletti, **Digital Design**, Fifth Edition, Pearson.

2) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010

3) Peter D Minns, **FSM-based digital design using Verilog HDL,** Chichester, England : J. Wiley & Sons , c2008

4) Pong P. Chu, **FPGA prototyping by Verilog examples Xilinx Spartan -3 version**, Hoboken, N.J. : J. Wiley & Sons, c2008

Grading: Part1 30%, Part2 70%

Note: *Submit your homeworks through Ninova.*