Improving Threshold Voltage and ON/OFF Current Ratio of Single-Walled Carbon Nanotube Field-Effect Transistor by Post-Sonication Treatments

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Abstract:

In the process of solution-based fabrication of Single-walled Carbon Nanotube Field Effect Transistor (SWCNT FET), the quality of SWCNTs network plays an important role. SWCNTs networks have disorders and defects because of chirality mismatches that cause the weaker tunneling between SWCNTs, hence suppressing conductance and the electrical performance of the device. In this paper, we present a study on the impact of SWCNTs network structure, which were formed in the channel on the prefabricated test chips, on electrical characteristic parameters like threshold voltage (V_T) and on/off current ratio (I_{ON}/I_{OFF}). Also, we propose a simple and low-cost post-process to decrease the V_T and enhance I_{ON}/I_{OFF} of SWCNT FET comparable to the reasonably good performances of the same devices to the date. Post-sonication treatments of the devices in the deionized water and the isopropyl alcohol not only removed the residual impurities remained between individual SWCNTs and around their surface and substrate, but also decreased the structural defects of their network (based on the provided Raman spectroscopy results). This improves I_{ON}/I_{OFF} up to 153 times and shifts V_T in the negative direction up to almost 0 V. The results indicate the importance of the improvement of SWCNTs network structure in enhancing SWCNT FET electrical performance.

1. Introduction

Carbon nanotubes (CNTs) have recently attracted great interest due to their high carrier mobility, good stability, and tunable band-gap structure with small diameter. Their applications have been proven to be

very successful in electronic devices such as field effect transistors (FETs), thin-films, optoelectronics and sensor systems [1–3].

CNTs are categorized into two groups of single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). There are two types of SWCNTs: metallic SWCNTs (m-SWCNTs) and semiconducting SWCNTs (s-SWCNTs). The s-SWCNTs are p-type semiconductors with the holes as the main charge carriers. The m-SWCNTs show metallic electronic properties. Both metallic and "ON" state semiconducting SWCNTs exhibit room temperature conductance near the ballistic transport limit of $4e^2/h$, where e is the electron charge and h is Planck's constant [4]. These properties of SWCNTs help to have high currents passing through SWCNTs without heating up the device. Generally, s-SWCNTs are preferred to use in the SWCNT FET devices [5].

Generally, there are three types of SWCNT FETs including metal oxide semiconductor field effect transistor (MOSFET) like SWCNT FETs, Schottky barrier SWCNT FETs, and tunneling SWCNT FETs. MOSFET-like SWCNT FETs are more capable to be implemented as electronic circuits because of their inherent electrical characteristics and transistor structure [6]. Fig. 1 shows a MOSFET-like SWCNT-FET structure. This device utilizes s-SWCNTs as the channel material instead of bulk silicon in the traditional MOSFET structure. The SWCNTs attached in the transistor channel enable a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [7]. Moreover, because of the large specific surface area in SWCNTs, which enables immobilization of a large number of functional units at the carbon nanotube surface, they were used to improve the signal-to-noise ratio in SWCNT FET-based biosensors [8]. SWCNT FET operates on the same principle of MOSFET as the electrons travel from the source terminal to the drain terminal [9]. They are being widely deliberated as probable replacement to silicon MOSFETs in last years. Since the miniaturization has always the key role in electronic evolution, SWCNT FET allows to obtain higher speed, lower power consumption, lower costs, and higher number of gates on chip in ultra-low-power and ultra-high-density integrated circuits [7,10]. While the MOSFET device characteristics and circuit behaviors change with the variations in temperature, it has been found that the effect of the temperature on threshold voltage of SWCNT FET is very low or negligibly small [9].

Threshold voltage (V_T) and on/off current ratio (I_{ON}/I_{OFF}) are two very important parameters in FETs. In digital logic, inaccurate V_T can lead jitter or a large short-circuit current during switching. Similarly, a poor I_{ON}/I_{OFF} can cause slow output transitions or impractically low output swings, while an appropriate I_{ON}/I_{OFF} can improve speed and minimize the leakage [10].

Solution-based deposition of s-SWCNT in FET channel is one of the widely used methods for the fabrication of SWCNT FET. In this method SWCNTs with different densities are dispersed in a solvent such as sodium dodecyl sulfate (SDS) which has great capability to disperse CNT into aqueous medium [11]. The obtained solution will be a composition of random SWCNTs network to be deposited in the

channel of a FET. Solution deposition methods including spin coating, spray coating, dip coating, electrophoretic deposition, and inkjet printing are currently being used for large-scale and low-cost manufacturing in different applications [12-14]. In the solution-based deposition method, electrical parameters of obtained SWCNT FET devices depend on the device geometry, material properties and fabrication process like the percentage of semiconducting part of used SWCNT, the method and material for surface treatment, solvent type, the SWCNT concentration in solvent, sonication energy (type and time), deposition type, heating treatment through the process, the morphology, disorder and impurity of the SWCNT network etc.

There are several experimental and theoretical works investigating the charge transport across the individual SWCNTs junctions [4,15]. However, the microscopic properties and their effects on the electronic properties of the interface region in SWCNTs networks are still unexplored. Inter-tube conductance in the network can be approximated accurately as tunneling between pairs of SWCNTs. Because of the chirality mismatches, the SWCNTs experience disorders and defects which cause weaker tunneling between the SWCNTs and therefore cause suppression in conductance and electrical performance of the device [15]. Therefore, the quality of SWCNT networks should be considered as an important parameter in the fabrication of such a device. There are some studies on the relationship between the quality of SWCNT networks and electrical properties of FETs [16-18] which mainly focus on the step of forming the networks on a FET rather than post fabrication modification on the already formed networks in the channel. In principle, aligned CNT arrays would provide better device performance, but it remains a challenge to obtain wafer-scale aligned CNT arrays with high uniformity [19]. When a prepared FET shows rather low I_{ON}/I_{OFF} due to network defects and tunneling issues between SWCNTs, the device is disposed of despite all the efforts, money and time spent during device fabrication. This risk can be mitigated by post treatment of SWCNT networks which are already formed in the channel of a FET. There is a study on post treatment of SWCNT networks formed on a FET channel which demonstrates a promising impact of sonication in deionized (DI) water on on/off current ratio of the SWCNT FET [20].

In this study, we present a simple post treatment process on an already deposited random SWCNT network on the channel of a FET to optimize both V_T and I_{ON}/I_{OFF} of the FET. The goal of this experiment-based study is to improve the quality and structure of SWCNTs network by removing the impurities like surfactant residuals and local disorders and defects of the network by post-sonication treatment process in DI-water and isopropyl alcohol (IPA). This process can also save the failed devices showing poor transistor characteristics due to its high density SWCNT network [20]. Therefore, researchers can save money and time.

2. Materials and Methods

In this work, prefabricated high-density test chips (Ossila Ltd) with empty channels, SiO_2 dielectric layers having 300 nm thickness, p-doped silicon substrates with Au gate (G) electrode which covers the conductive edge of the substrate, Au drain (D) and source (S) electrodes were used. Test chips have 70 nm gold electrodes and 2 nm chromium is used beneath the gold as adhesion layer. The channel length (L) is 30 μm, and the channel width (W) is 1 mm. Fig. 1 presents the top view of the purchased prefabricated test chip and illustrates the simplified schematic structure of the bottom gate bottom contact (BGBC) SWCNT FET. SWCNTs used in this study were synthesized by high-pressure catalytic carbon monoxide (HiPco) decomposition (HiPco, 95 % semiconducting, 1.0 ± 0.2 nm) that were purchased from NanoIntegris Inc.

For the first step, the test chip was immersed into diluted 3-Aminopropyl triethoxy silane (APTES) solution (1 % APTES in DI-water) for 10 minutes to functionalize the substrate and to increase the surface wettability. Following by that, the sample was rinsed with water, blown dry and annealed at 100 °C for 30 minutes. The solution which includes 0.03 mg/mL semiconducting carbon nanotubes (95 % semiconducting single-walled carbon nanotube, NanoIntegris Inc.) in DI-water with 1 wt % SDS was obtained by 30 min sonication at 15 Wcm^{-2} power density (Bandelin Sonopuls ultrasonic homogenizer). In order to prevent heating during the process, the bottle containing the sample solution was immersed in a bath of cold water (5-10 ℃) consequently. Then, SWCNTs-solution were spin-coated over the pre-treated test chips to fill the transistor channel. Five cycles of spin-coating were performed with 60 seconds at 1500 rpm for each layer. In the next step, the chips were rinsed by IPA and DI-water then were dried at 100 °C for 1 hour. As the final step, sonication bath treatments were applied for two chips, one placed in IPA and other in DI-water for 40, 80 and 120 min (increasing by steps of 40 min).

The current-voltage characteristics of all devices before and after each sonication process were measured by Agilent B1500A semiconductor parameter analyzer. Electrical measurements were carried out on a device by sweeping the gate-to-source voltage (V_{GS}) from + 10 to – 10 V in steps of – 1 V for each drain-to-source voltage (V_{DS}), swept from 0 to – 10 V in steps of – 1 V.

In order to evaluate the quality of SWCNTs network structure, Scanning Electron Microscopy (SEM, Jeol JSM-6010LV, operated at 15 kV) and micro-Raman spectroscopy (Renishaw inVia Raman, laser excitation at 532 nm) were performed for the SWCNTs network channel between the source and drain electrodes.

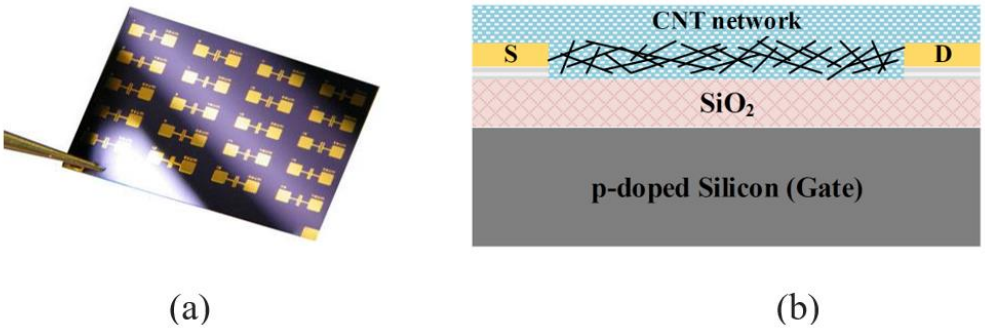

Fig. 1. (a) Top view of the prefabricated test chip [Image remains the copyright of Ossila Ltd. Taken with permission from Ossila.com] and (b) simplified schematic structure of BGBC SWCNT FET. Note that gate electrode which covers conductive edge of the substrate is not shown for the sake of clarity.

3. Result and Discussion

Measurement results of SWCNT FET generally depend on device geometry, fabrication details and test conditions. Fabrication related parameters in solvent-based SWCNT FET can be defined by a number of parameters including (but not limited to) the percentage of semiconducting SWCNTs, the method and material for surface treatment, solvent type, the SWCNTs concentration in solvent, sonication energy for mixing the SWCNTs (type and time), deposition type, heating treatment through the process, the morphology, bundle alignment and disorders or impurity of the SWCNTs network. After optimizing almost all of the mentioned process parameters, we focused on optimizing the quality of SWCNTs network by monitoring the effect of bath sonication treatments in IPA and DI-water which were applied by placing the chips in sonication bath for 40, 80 and 120 min (in the electrical measurements the best duration was 80 min). During the measurement, by keeping the device geometry and test conditions fixed, the electrical characteristic parameters of SWCNT FET have been investigated.

Although individual SWCNTs have specific semiconducting or metallic electronic properties, SWCNTs networks do not have specific electronic properties. This is due to their different inter-tubular contact resistance; the contact points act essentially as tunneling junction for electrons that are very sensitive to distance. The efficacy of impurities and disorders are based on acting as a spacer between tubes and at metal-nanotube contacts, so any additional distance in network is detrimental to the electronic characteristics due to the decrease in the band-to-band tunneling current. This current is also reduced by the presence of insulating SDS among the cross junctions [21].

Thanks to post-sonication treatments in IPA and DI-water, beside purifying the network by removing additional particles (like SDS) between nanotubes, a substantial decrease in the defects of SWCNTs network was observed in the Raman spectra as shown in Fig. 7. In the process, although the chips were rinsed by IPA and DI-water to wash out the solvent after spin coating and baked at 100 °C for 1 hour, some residual SDS still remained around the SWCNTs bundles, as shown in Fig. 2a and 2c. It was obvious that

after 80 min sonication in DI-water process this amount has been reduced, more over the sonication in DI-water formed a sparse network by eliminating a large number of SWCNTs from the pristine network, as shown in Fig. 2b.

Also, we observed a parallel aligned network after 80 min sonication in IPA as shown in Fig. 2d. The electrical conductivity of the SWCNTs network correlates with the orientation of the SWCNTs in the network, they exhibit higher resistance in randomly-aligned networks compared to the parallel aligned ones [22]. This issue is in good agreement with the experimental result seen in Table 1, strongly supporting that the enhanced on/off current ratio of the FET is due to a parallel aligned SWCNTs network realized by 80 min sonication in IPA.

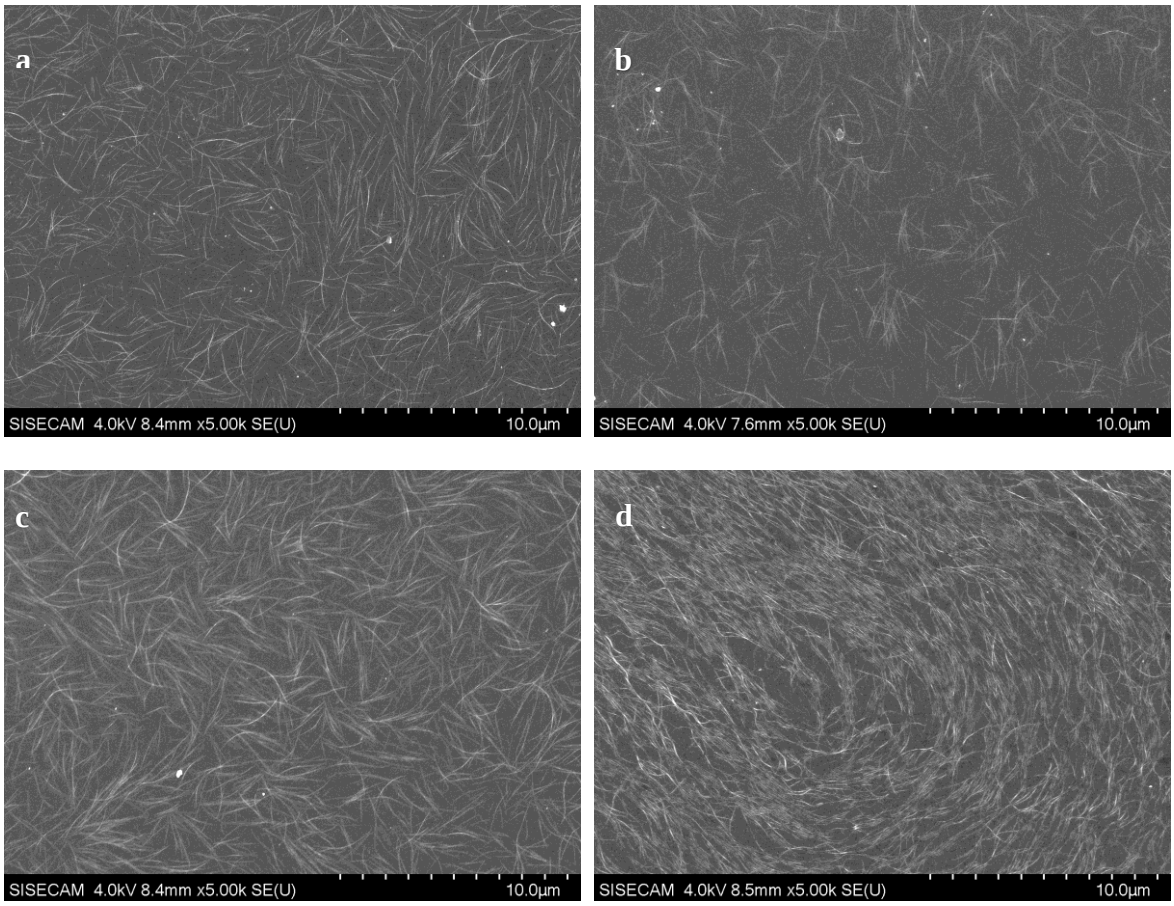

Fig. 2. SEM images of SWCNTs network (a) before sonication in DI-water, (b) after 80 min sonication in DI-water, (c) before sonication in IPA, (d) after 80 min sonication in IPA.

Table 1 The calculated V_T and I_{ON}/I_{OFF} parameters of SWCNT FETs before and after sonication

Transistor code		**Process**	**in IPA (Chip A)**		**in DI-Water (Chip B)**	
IPA	**DI-Water**		**V_T (V)**	**I_{ON}/I_{OFF}**	**V_T (V)**	**I_{ON}/I_{OFF}**
A1	B1	Before Sonication	5.09	8756	4.02	33517
		After 40 min Sonication	2.20	11197	2.88	45162
		After 80 min Sonication	2.48	1339397	2.75	283692
		After 120 min Sonication	4.20	124161	4.75	44025
A2	B2	Before Sonication	4.84	8692	7.51	431
		After 40 min Sonication	3.41	13738	5.69	1656
		After 80 min Sonication	3.52	194649	0.28	54893
		After 120 min Sonication	4.72	35921	5.75	2925
A3	B3	Before Sonication	6.79	6123	3.34	8988
		After 40 min Sonication	5.29	14614	2.08	30334
		After 80 min Sonication	3.76	83446	2.28	67318
		After 120 min Sonication	4.42	20958	3.94	13540
A4	B4	Before Sonication	7.50	301	4.01	10787
		After 40 min Sonication	4.33	3839	3.39	33405
		After 80 min Sonication	3.04	4869	3.35	231644
		After 120 min Sonication	3.82	911	4.11	46144
A5	B5	Before Sonication	4.01	7747	4.13	17456
		After 40 min Sonication	3.19	9695	2.85	33591
		After 80 min Sonication	2.35	55067	2.46	74623
		After 120 min Sonication	2.36	29378	3.10	23131
A6	–	Before Sonication	8.45	46	–	–
		After 40 min Sonication	6.75	457	–	–
		After 80 min Sonication	5.44	5858	–	–
		After 120 min Sonication	6.68	873	–	–

Table 1 shows the threshold voltages and on/off current ratios calculated for the transistors before and after sonication processes. There are, respectively, 5 and 6 transistors' data that could be obtained after all sonication steps in DI-water and in IPA. Some of the devices did not show transistor behavior due to possible defects, such as pin holes and comet streaks, known for spin coating method and some of them lost the transistor characteristic curves after 120 min sonication process. The remaining transistors' data were used for the calculations of V_T and I_{ON}/I_{OFF}. The transistors showing the highest I_{ON}/I_{OFF} ratio after sonication processes in IPA and DI-water were selected to show their characteristic curves and application of threshold voltage extraction method. Maximum transconductances of SWCNT FET are found between 19 nS and 284 nS before sonication process, however we did not observe any significant change after sonication process or a certain trend for the transconductance with respect to sonication time.

Fig. 3 and Fig. 4 show the transfer characteristics (I_D–V_{GS} curves) of the SWCNT FET, labelled as A1 and B1, before and after sonication processes in IPA and DI-water, respectively. The performance metrics such as V_T and I_{ON}/I_{OFF} are calculated using these characteristic curves. Threshold voltage is the minimum voltage required to be applied at the gate terminal of a FET device to turn it on. V_T is extracted from I_D–V_{GS} data using linear extrapolation technique [23] with drain current equation of MOSFET in the linear regime given as follows:

$$I_D = \frac{W}{L}\mu_{FET}C_{ox}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS} \quad (1)$$

where μ_{FET} is the field-effect mobility, C_{ox} is the oxide capacitance (~10.9 nF/cm^2). The transistor operates in linear regime for low V_{DS} voltages and (1) is valid only above threshold voltage. The drain current is asymptotically approaching zero below V_T.

In linear extrapolation technique, I_D-V_{GS} data, measured for low V_{DS}, is extrapolated to zero drain current and V_T is calculated from the interception point (V_{GSi}) on V_{GS}–axis. According to (1), I_D is zero when V_{GS} is equal to ($V_T + 0.5V_{DS}$). Hence V_T can be calculated as follows:

$$V_T = V_{GSi} - V_{DS}/2 \quad (2)$$

Fig. 5 and Fig. 6 show the application of this threshold voltage extraction technique for the transistors A1 and B1 before and after sonication processes in IPA and DI-water, respectively. V_T was found as 5.09 V before sonication for the transistor A1. The same transistor was exposed to sonication processes in IPA for 40 min, 80 min, and 120 min. After 40 min sonication, V_T was decreased to 2.20 V and it was nearly 57 % improvement. After 80 min sonication V_T was calculated as 2.48 V and this is still a significant improvement. However, V_T got worse for 120 min sonication, comparing to the previous ones. The other transistor B1 was exposed to sonication processes in DI-water for 40 min, 80 min, and 120 min. When it was analyzed, V_T was initially found as 4.02 V before sonication and it was improved after 40 min and 80

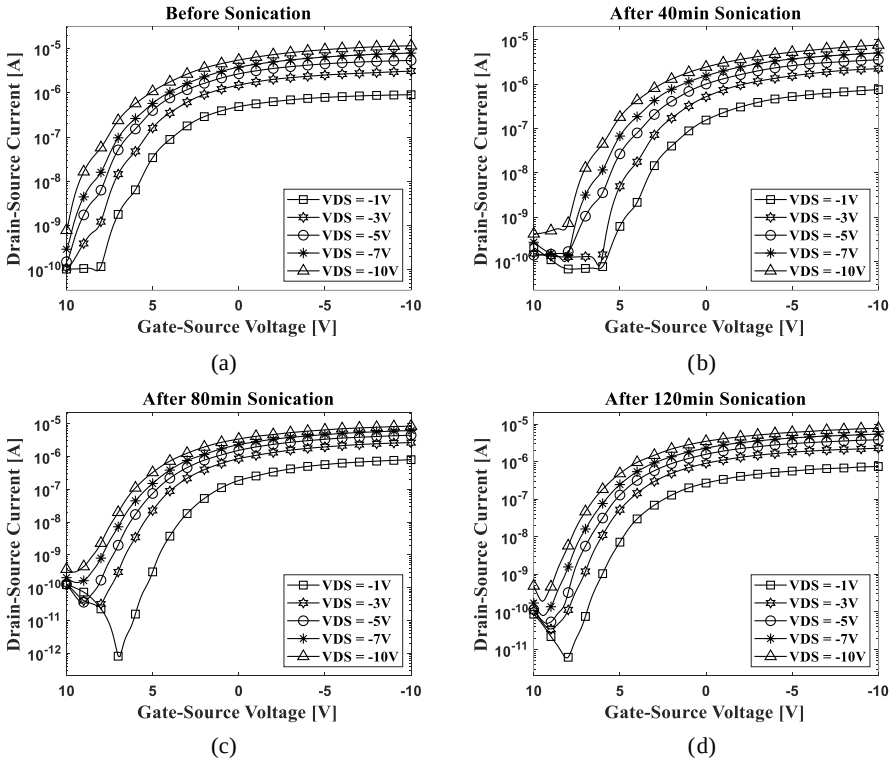

Fig. 3. Transfer characteristic (I_D–V_{GS}) curves of the transistor A1 for (a) before sonication, (b) after 40 min sonication in IPA, (c) after 80 min sonication in IPA, (d) after 120 min sonication in IPA.

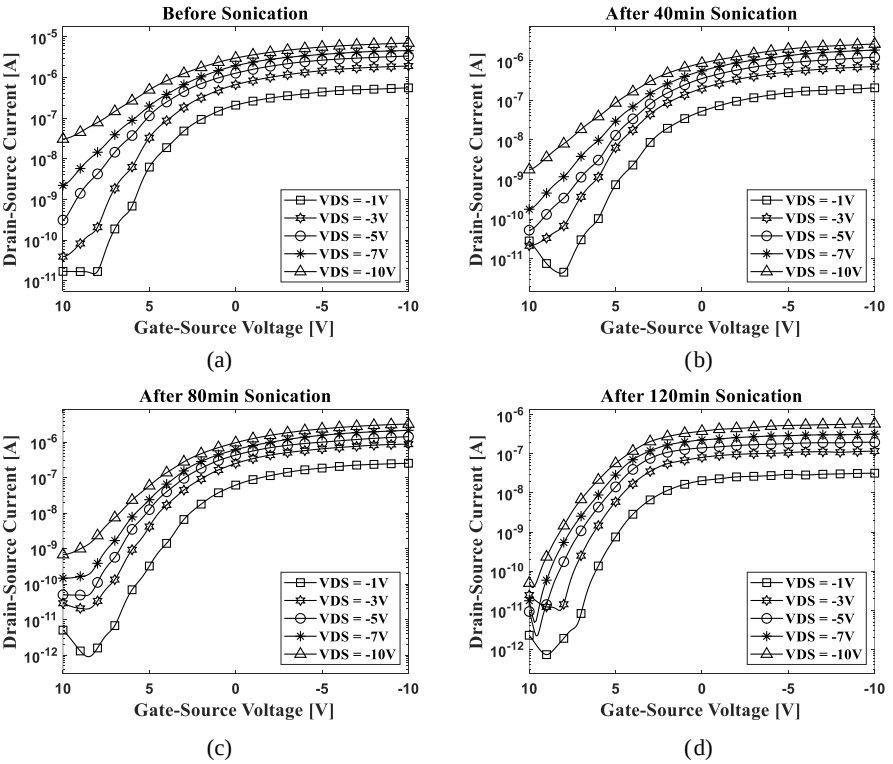

Fig. 4. Transfer characteristic (I_D–V_{GS}) curves of the transistor B1 for (a) before sonication, (b) after 40 min sonication in DI-Water, (c) after 80 min sonication in DI-Water, (d) after 120 min sonication in DI-Water.

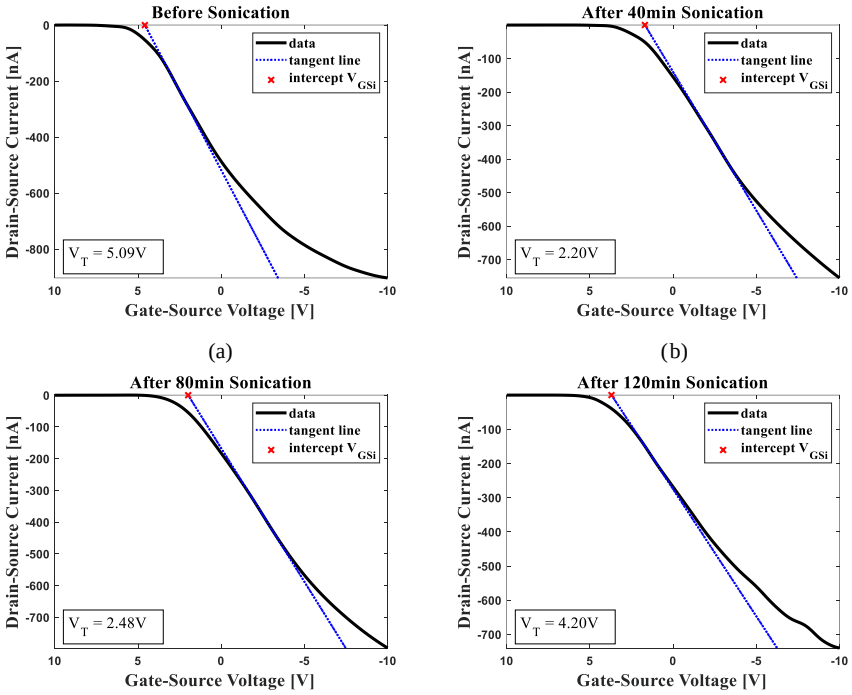

Fig. 5. Threshold voltage extraction from I_D-V_{GS} curve when V_{DS} = – 1 V using linear extrapolation technique for (a) before sonication, (b) after 40 min sonication in IPA, (c) after 80 min sonication in IPA, and (d) after 120 min sonication in IPA for the transistor A1.

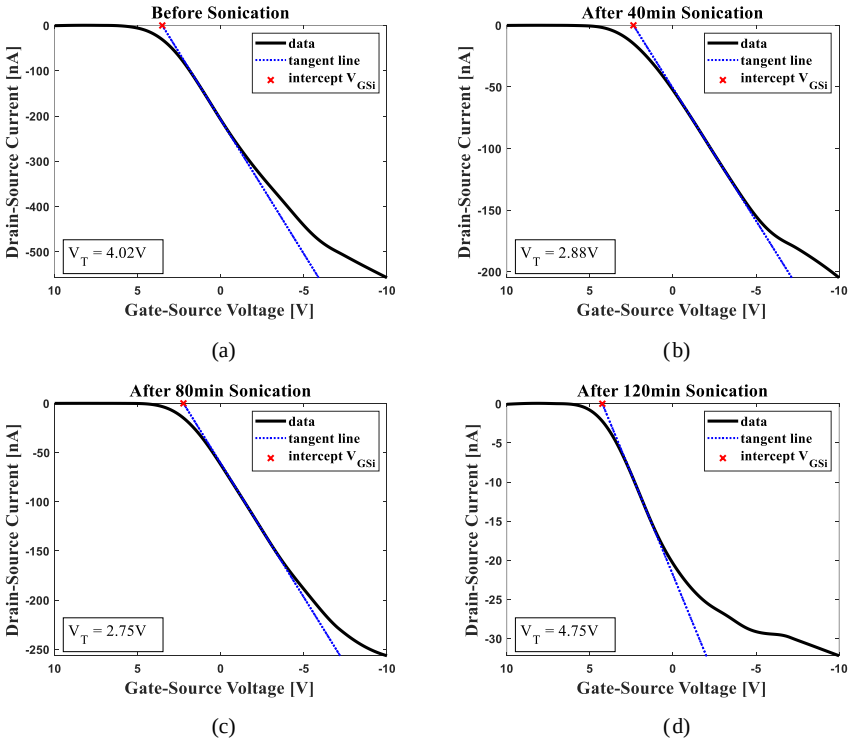

Fig. 6. Threshold voltage extraction from I_D-V_{GS} curve when V_{DS} = – 1 V using linear extrapolation technique for (a) before sonication, (b) after 40 min sonication in DI-water, (c) after 80 min sonication in DI-water, and (d) after 120 min sonication in DI-water for the transistor B1.

min sonication processes. V_T was calculated as 2.75 V after 80 min sonication, and this was 32 % improvement for the threshold voltage. After 120 min sonication, no improvement was observed; moreover, V_T got even worse compared with the one before sonication. Table 1 presents calculated V_T for all the transistors before and after sonication in IPA and DI-water for each time step. As seen from the calculated threshold voltages of the other transistors, we could observe the same improvement trend up to 80 min sonication process both in IPA and DI-water. For instance, the improvements in threshold voltages are 27 % and 96 % for A2 and B2, 45 % and 32 % for A3 and B3, 59 % and 16 % for A4 and B4, 41 % and 40 % for A5 and B5, and 36 % for A6 after 80 min sonication processes in IPA and DI-water, respectively. We did not observe any further improvement after 120 min sonication processes in both cases, because excessive sonication gives damage to SWCNTs and converts crystalline graphene layers of SWCNTs into amorphous carbon [24, 25] and accordingly, it generates defects and impurities that lead to threshold voltage shifts in the positive direction. These results are agreed with [26] that sonication helps enhancing electrical properties of SWCNTs to an optimal level and excessive sonication deteriorates that corresponding properties.

On the other hand, on/off current ratio was also calculated from the transfer characteristics. In the literature, maximum I_{ON}/I_{OFF} is often reported. We calculated this performance metric similar to [10] as follows:

$$\frac{I_{ON}}{I_{OFF}} = \frac{I_{D,max}}{I_{D,min}}, \qquad when \;\; V_{DS} = -1\,V \tag{3}$$

The first SWCNT FET devices, labelled as A1 and B1, respectively exhibited on/off current ratios of 8756 and 33517 before sonication. After proposed sonication treatments, an enhancement in I_{ON}/I_{OFF} was observed. While the on/off current ratio was enhanced by 153 times after 80 min sonication in IPA, it was enhanced by only 8.5 times in DI-water for the same sonication time. It was observed that the on/off current ratios decreased for 120 min sonication. Table 1 also presents calculated I_{ON}/I_{OFF} ratios of all the transistors before and after sonication in IPA and DI-water for each time step. As seen from the table, the highest I_{ON}/I_{OFF} ratios are calculated after 80 min sonication process in each case without any exception and we also observed a decline in these ratios after 120 min sonication process.

The effect of sonication in IPA and DI-water can be examined from the results in Table 1. The threshold voltage shift is related to reducing the defects and impurities of SWCNT network in the channel using sonication treatment for an appropriate time. The most significant improvement in V_T was observed after 40 min and 80 min sonication in IPA and DI-water. While two out of six transistors in the chip A showed better V_T after 40 min sonication, the other four transistors showed better V_T after 80 min sonication in IPA. The best V_T values calculated for the transistors A1 and A2 after 40 min sonication were very close to those

calculated for the same transistors after 80 min sonication. However, improvements in V_T could be observed up to 30 % for the transistors A3 – A6 after 80 min sonication with respect to the results after 40 min sonication. In DI-water, four out of five transistors of the chip B showed better V_T after 80 min sonication. The other transistor labelled as B3 showed the best V_T after 40 min sonication, but the relative difference between the results after 40 min and 80 min sonication processes was below 10 %. On the other hand, a sonication process for an appropriate time can decrease the leakages in the channel and off currents could be measured as a few pico-amps in this experiment. The most significant improvements in I_{ON}/I_{OFF} ratios were observed after 80 min sonication in IPA and DI-water for all the transistors of the chips A and B. It was also pointed out that 120 min sonication negatively affects these parameters. After all, 80 min sonication was observed as the most effective process among all. Besides, the best enhancement in I_{ON}/I_{OFF} and also the highest value of this ratio was seen in IPA for A1 and the most significant improvement in V_T and the lowest value of this parameter was seen in DI-water for B2. Hence, it was experimentally shown that electrical characteristics could be improved using 80 min post-sonication process in either of IPA or DI-water.

The electrical anisotropy measurement indicates impurities and defects in SWCNTs network that distinguishes by Raman scattering technique which provides macroscopic characterization of the structure of SWCNTs network. The presence of amorphous carbon or other impurities could have a shielding effect on the Raman intensity of SWCNTs. Fig. 7 shows the micro-Raman spectra of the SWCNTs network channel before and after sonication for both of DI-water and IPA. Three characteristic peaks were observed for each spectrum. One peak at approximately 530 cm^{-1} is Radial Breathing Mode (RBM), carbon atoms vibrate in the radial direction of tube axis in RBM mode, as if the nanotube was breathing, therefore it is called RBM. This relationship is described as: $\omega(RBM) = 219.3/d + 14.7$, where d is the diameter of carbon nanotube. Another peak at approximately 1590 cm^{-1} is the G-band that originates from the SWCNTs structure. The other peak at approximately 1340 cm^{-1} is the D-band that is related to structural defects, disorders and impurities such as amorphous carbon. So, the D-band to G-band intensity ratio (D/G ratio) indicates the amount of defects and impurities in the SWCNTs network [27]. D/G ratio of the SWCNTs network channel before sonication was about 0.1, After 80 min sonication in DI-water and IPA, this amount decreased to 0.05 and 0.02, respectively. Based on the micro-Raman spectroscopy results, it can be inferred that the network structural changes were resulted by sonication process in both of DI-water and IPA. Less defected and more aligned network means higher contact area of nanotubes, less distance and stronger tunneling between them, leading to decrease in the V_T and increase in the I_{ON}/I_{OFF}. In particular, the electrical properties of the SWCNTs network transistor depend dominantly on the contact resistance of the SWCNTs segment [28,29].

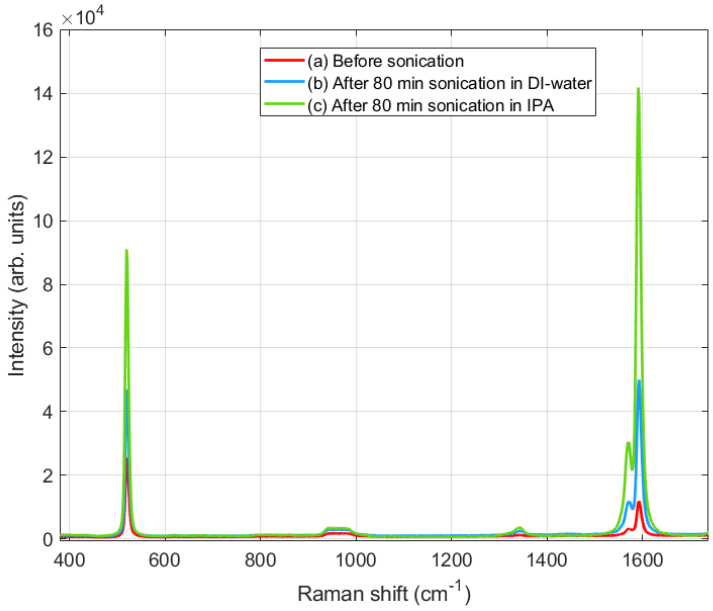

Fig. 7. Micro-Raman spectra of the SWCNTs network between the source and drain electrodes (a) before sonication, (b) after 80 min sonication in DI-water, (c) after 80 min sonication in IPA

4. Conclusion

In this study, we demonstrated a post-sonication treatment process to decrease the defects and impurities of the SWCNTs network formed in the channel of a prefabricated test chip. Microscopic analysis clearly showed that SWCNTs network in the channel can be influenced by post-sonication process where in DI-water, it decreases the defects and impurities of SWCNTs network with a sparse network. On the other side, in IPA as well as reducing the defects and impurities of the network, a more uniform and directive orientated network was observed. From the experimental results, both I_{ON}/I_{OFF} and V_T were improved by post-sonication process in DI-water and IPA for 80 min. The higher I_{ON}/I_{OFF} after sonication in IPA can be related to network orientation of the SWCNTs. The presented approach may find use in solution-based SWCNT nano-device fabrication methods to enhance quality of the SWCNTs network which leads to improvement in the characteristic parameters of SWCNT FET.

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