

# EHB322E Digital Electronic Circuits QUIZ I

Duration: 60 Minutes

Grading: 1) 50%, 2) 50%

For your answers please use the space provided in the exam sheet

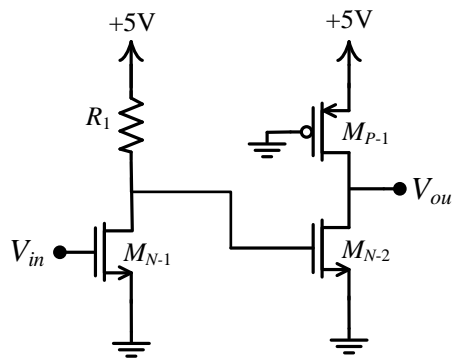
**GOOD LUCK!**

- 1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation:  $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0p,n})^2$

Linear region current-voltage equation:  $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} [2(V_{GS} - V_{T0p,n})V_{DS} - V_{DS}^2]$

Transistor parameters:  $k_p' = \mu_p C_{ox} = 54 \mu A/V^2$ ,  $k_n' = \mu_n C_{ox} = 96 \mu A/V^2$ ,  $V_{TN} = 1V$ ,  $V_{TP} = -1V$ ,  $W_{N-1} = W_{N-2} = 12 \mu$ ,  $L_P = L_N = 1 \mu$ .



Buffer

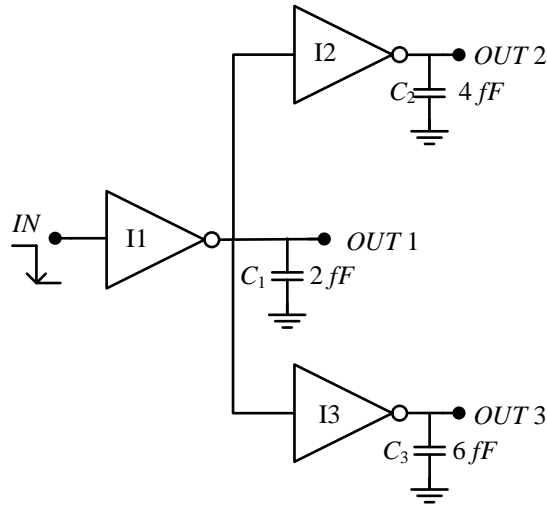
- Find the minimum value of  $R_1$  if  $V_{in} = 5V$  results in  $V_{out} = 5V$ .
- Find the value of  $W_{P-1}$  if  $V_{in} = 0V$  results in  $V_{out} = 0.5V$ .
- Find the buffer's static power consumption values when  $V_{in} = 0V$  and  $V_{in} = 5V$ .

a)  $V_{G2} = 1V \Rightarrow M_2$  is in linear region  
 $I_{DN-1} = \frac{1}{2} \cdot 96 \cdot 12 \cdot [2 \cdot (4) \cdot 1 - 1] = 4,032 \mu A$  (20)  
 $\Rightarrow R_1 = (5V - 1V) / I_{DN-1} \approx 1k\Omega$

b)  $V_{G2} = 5V \Rightarrow M_2$  is in linear region  
 $M_{P1}$  is in sat. region  
 $V_{out} = 0.5V$   
 $\Rightarrow \frac{1}{2} \cdot 54 \cdot W_{P-1} \cdot (4 - 0.5)^2 = \frac{1}{2} \cdot 96 \cdot 12 \cdot [2 \cdot (4) \cdot 0.5 - 0.5^2] \Rightarrow W_{P-1} = 5 \mu$  (20)  
 $I_{DN-2} = 2,16 \mu A$   
 $I_{DP-1}$

c)  $V_{in} = 0V \Rightarrow SP = 2,16 \mu \cdot 5V \approx 10,8 mW$   
 $V_{in} = 5V \Rightarrow SP = I_{DN-1} \cdot 5V \approx 20 mW$  (10)

- 2) Consider a circuit with three CMOS inverters and three outputs shown below. External capacitors with values of  $2fF$ ,  $4fF$ , and  $6fF$  are connected to output-1, output-2, and output-3, respectively. A signal switching from high to low is applied to the input. Transistor parameters:  $c_{ox}=1 fF/\mu m^2$ ,  $\tau_n = \tau_p=1ps$ ,  $W_{N1}=2\mu$ ,  $W_{P1}=4\mu$ ,  $W_{N2}=2\mu$ ,  $W_{P2}=6\mu$ ,  $W_{N3}=1\mu$ ,  $W_{P3}=4\mu$ , and  $L_{N1}=L_{P1}=L_{N2}=L_{P2}=L_{N3}=L_{P3}=1\mu$ .



Digital circuit with three CMOS inverters

Propagation delays of an inverter are formulized as follows.  $C_L$  represents the total (internal and external) load capacitor of an inverter.

$$t_{PHL} = (C_L/C_N) \tau_n \quad C_N = c_{ox} W_N L_N$$

$$t_{PLH} = (C_L/C_P) \tau_p \quad C_P = c_{ox} W_P L_P$$

- a) Neglect the inverters' internal output capacitors and find **total propagation delay values** at output-1 (delay of I1), output-2 (delay of I1+delay of I2), and output-3 (delay of I1+delay of I2).
- b) Suppose that each inverter has an input internal capacitor  $C_{I-in} = c_{ox}(W_N+W_P)(1\mu m)$  and an output internal capacitor  $C_{I-out} = c_{ox}(W_N+W_P)(0.5\mu m)$ . Find **total propagation delay values** (by considering both internal and external capacitors) at output-1, output-2, and output-3.

⑩ for writing  $t_{PD}$  equations

a)  $t_{PD-1} = t_{PLH1} = \frac{C_L}{C_P} \tau_p$   $C_L = 2f + 4f + 6f = 12f$   
 $C_P = 4f$   
 $\Rightarrow t_{PD-1} = \frac{12}{4} 1ps = 3.75ps$

⑤  $t_{PD-2} = t_{PLH1} + t_{PHL2}$   $t_{PHL2} = \frac{C_L}{C_N} \tau_n \Rightarrow t_{PHL2} = 2ps$   
 $C_L = 4f$   $C_N = 2f$

⑤  $= 5.75ps$

⑤  $t_{PD-3} = t_{PLH1} + t_{PHL3}$   $t_{PHL3} = \frac{6}{1} ps$

⑤  $= 9.75ps$

b) ⑩ for writing the equations

⑤  $t_{PD-1} = t_{PLH1} = \frac{2+3+8+5}{4} ps = 4.5ps$

⑤  $t_{PD-2} = t_{PLH1} + t_{PHL2} = 4.5ps + \frac{8}{2} ps = 8.5ps$

⑤  $t_{PD-3} = t_{PLH1} + t_{PHL3} = 4.5ps + \frac{8.5}{1} ps = 13ps$