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EHB322E Digital Electronic Circuits
MIDTERM I

Duration: 120 Minutes

Grading: 1) 35%, 2) 35%, 3) 30%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

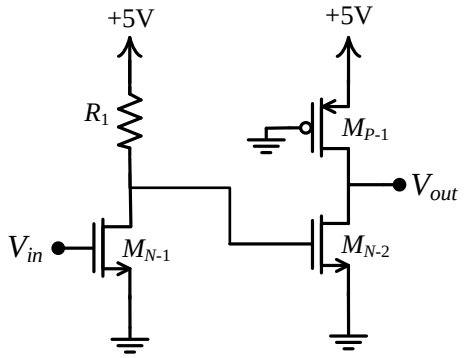
GOOD LUCK!

1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0\,p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} \left[2(V_{GS} - V_{T0\,p,n})V_{DS} - V_{DS}^2\right]$

Transistor parameters: $k_p' = \mu_p c_{ox} = 54\text{uA/V}^2$, $k_n' = \mu_n c_{ox} = 96\text{uA/V}^2$, $V_{TN} = 1\text{V}$, $V_{TP} = -1\text{V}$, $W_{N-1} = W_{N-2} = 12\text{u}$, $L_P = L_N = 1\text{u}$.



Buffer

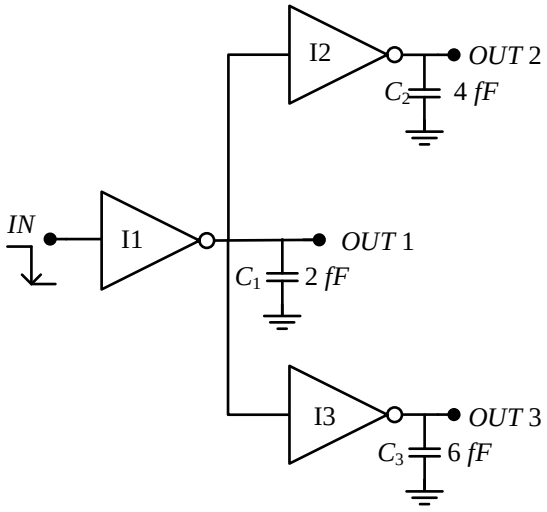
a) Find the minimum value of $\boldsymbol{R_1}$ if $\boldsymbol{V_{in}}$**=5V** results in $\boldsymbol{V_{out}}$**= 5V**.

b) Find the value of $\boldsymbol{W_{P-1}}$ if $\boldsymbol{V_{in}}$**=0V** results in $\boldsymbol{V_{out}}$**= 0.5V**.

c) Find the buffer's static power consumption values when $\boldsymbol{V_{in}}$**=0V** and $\boldsymbol{V_{in}}$**=5V.**

d) Using the values found in a) and b), find the value of $\boldsymbol{V_{out}}$ if $\boldsymbol{V_{in}}$**=2.5V**.

2) Consider a circuit with three CMOS inverters and three outputs shown below. External capacitors with values of 2*fF*, 4*fF*,and 6*fF* are connected to output-1, output-2, and output-3, respectively. A signal switching from high to low is applied to the input.
Transistor parameters: c_{ox}=1 *fF*/um^2, $\tau_n = \tau_p$=1ps, W_{N1}=2u, W_{P1}=4u, W_{N2}=2u, W_{P2}=6u, W_{N3}=1u, W_{P3}=4u, and L_{N1}=L_{P1}= L_{N2}= L_{P2}= L_{N3}= L_{P3}=1u.



Digital circuit with three CMOS inverters

Propagation delays of an inverter are formulized as follows. C_L represents the total (internal and external) load capacitor of an inverter.

$t_{PHL} = (C_L/C_N)\,\tau_n$ $\quad C_N = c_{ox}W_NL_N$

$t_{PLH} = (C_L/C_P)\,\tau_p$ $\quad C_P = c_{ox}W_PL_P$

Suppose that $C_{GS\text{-}N} = C_N$, $C_{GS\text{-}P} = C_P$, and each inverter has an internal input capacitor of $(C_{GS\text{-}N} + C_{GS\text{-}P})$.

a) Neglect the inverters' internal output capacitors and find **total propagation delay values** at output-1, output-2, and output-3.

b) Suppose that each inverter has an output internal capacitor $C_{I\text{-}out} = c_{ox}(W_N+W_P)(0.5um)$. Find **total propagation delay values** at output-1, output-2, and output-3.

3) Consider $f = x_1x_2x_3\overline{x_4} + x_1x_2\overline{x_3}x_4 + \overline{x_1}\,\overline{x_2}\,\overline{x_3}x_4$.

a) Implement f with a **CMOS circuit** using **minimum** number of transistors. Draw the circuit. How many PMOS and NMOS transistors do you use?

b) Suppose that both NMOS and PMOS transistors have equivalent resistance values of 1kΩ; a total output load capacitor is 2 *fF* (Neglect all other internal capacitors). Find the **worst case (largest)** t_{PHL} and t_{PLH} values.