Synthesis and Performance Optimization of a Switching Nano-Crossbar Computer

General Overview
- 1963, 1965: CMOS and Moore’s Law
- 2005: Gordon Moore himself claimed that the validity of Moore’s Law will be lost.
- February 2016: Mitchell Waldrop stated: “Next month, the worldwide semiconductor industry will formally acknowledge … Moore’s law … is nearing its end.”
- Novel fabrication methods like self-assembly
- Regular shaped Crossbar structures

Crossbar-Switch Types
There are three different types of nano crossbar switches:
- Diode type
- FET type
- Four-terminal type

4x4 pseudo-nMOS ROM Example

Arithmetic Logic Synthesis Examples
- Diode type
- FET type
- Four-terminal type

# of Switch Optimization Example
For Four-terminal switch type

Defect Tolerant Mapping

These three network designs realize the same function XOR3; but smallest network is the optimal solution for this function

Project Goal
- Synthesis and optimization methodology for switching nano-crossbar arrays: diode, FET, and four-terminal switch based
- Performance parameters such as area, delay, power dissipation, and reliability
- New computing models arithmetic and memory elements
- Realization of a synchronous state machine (SSM) with combination of arithmetic and memory elements

Project Partners
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- Prof. Mehdi B. Tahoori, Dependable Nano-Computing Group, Karlsruhe Institute of Technology, Germany

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