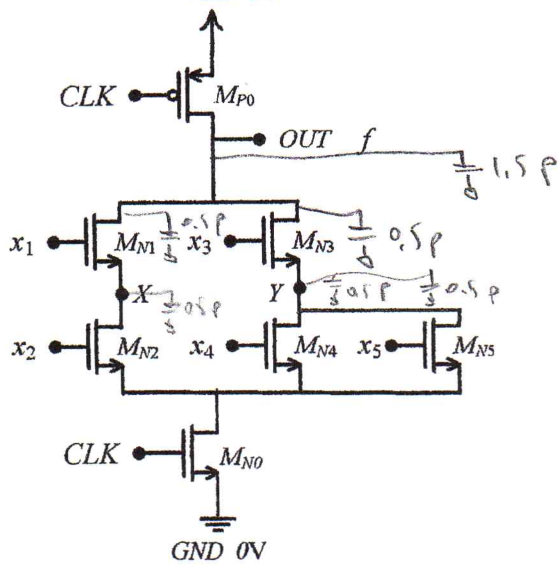
- Suppose that each transistor has an internal grounded gate capacitor C_G and drain capacitor C_D:
  $C_G = c_{ox} W L$; $C_D = (c_{ox} W L)/2$; c_{ox}=1 pF/um^2.
- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
- $W_{N0}=W_{N1}=W_{N2}=W_{N3}=W_{N4}=W_{N5}=1u$, $W_{P0}=3u$, and $V_{TN}=|V_{TP}|=1V$.



Dynamic Logic Circuit

a) Derive a Boolean expression of f in terms of the inputs x_1 through x_5 in evaluation phase.

b) At the start of the evaluation phase suppose that $x_1 = 0 \rightarrow 1$, $x_2 = 0$, $x_3 = 0 \rightarrow 1$, $x_4 = 0$, $x_5 = 0$, and V_X = 0V, V_Y = 0V, V_{OUT} = 5V. Considering the charge share problem, find the final voltage value at the output.

c) To make the final voltage value at the output as 4.5V, determine the capacitor value of a load to drive.

(20) a) $f = \overline{(x_1 x_2 + x_3(x_4+x_5))}$ — 20

b)

$C_L = 1.5p + 0.5p + 0.5p = 2.5p$

$C_X = 0.5p$ $\quad C_Y = 1p$

- Assume that $OUT_{final} \geq (V_{DD} - V_T)$, $X_{final} = 4V$, $Y_{final} = 4V$
4V

(50) $\Rightarrow 4V \cdot 0.5p + 4V \cdot 1p \leq 2.5p \cdot 1V$ ✗ assumption is wrong — 25

$\Rightarrow OUT_{final} = X_{final} = Y_{final} = V_f < 4V$

$(2.5p) \cdot (5 - V_f) = 1p \cdot V_f + 0.5 \cdot V_f$

$\Rightarrow 12.5 = 4p\, V_f \Rightarrow V_f = 3.125V$ — 25

(30) c) $(5-4.5)\, C_L = 4 \cdot 0.5p + 4 \cdot 1p \Rightarrow C_L = 12p$ — Addl cap = 9.5p — 15

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