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EHB205E Introduction to Logic Design
Homework 2

Deadline: 29/01/2021 (submit via Ninova before 9:30)

1) Create a new project as explained in your first homework.
2) Write a VHDL code for an AND gate.
3) Add your "*.vhd" by "Add Sources", "Add or create design sources" to your project.
4) Make sure that "*.vhd" is your top module. You can change top module by right click to the module that you would like to implement and choose "Set as Top" from the list. Produce the RTL schematic of your AND gate.
5) Write a "*_tb.vhd" as a testbench and add "*_tb.vhd" to your project by "Add Sources", "Add or create simulation sources" to your project.
6) Simulate your AND gate.
7) Write a VHDL code for a NOT gate.
8) Add your "*.vhd" by "Add Sources", "Add or create design sources" to your project.
9) Make sure that "*.vhd" is your top module. Produce the RTL schematic of your NOT gate.
10) Write a "*_tb.vhd" as a testbench and add "*_tb.vhd" to your project by "Add Sources", "Add or create simulation sources" to your project.
11) Simulate your NOT gate.
12) Add your "OR_gate.vhd" by "Add Sources", "Add or create design sources" to your project.
13) You will implement Boolean function $f(x,y,z,t,w) = \sum 0,10,13,14,15,18,24,28,29 + d\sum 2,16,31$ using AND, OR and NOT gates. Simlify the given Boolean function using Quine-McCluskey method.
14) Draw your circuit for the simplified Boolean function.
15) Write the VHDL code for the simplified Boolean function using structural modelling. Describe your AND, OR and NOT gates as sub-components. You can find some examples fro structıural modelling w,th VHDL at the following links.
https://www.doulos.com/knowhow/vhdl_designers_guide/components_and_port_maps/
http://www.csit-sun.pub.ro/courses/Masterat/Xilinx%20Synthesis%20Technology/toolbox.xilinx.com/docsan/xilinx4/data/docs/xst/vhdl7.html
https://mil.ufl.edu/3701/examples/vhdl/VHDL_examples.pdf
16) Make sure that the VHDL code for the simplified Boolean function is your top module. Produce the RTL schematic of your design.
17) Write the test bench file to test the VHDL code for the simplified Boolean function. Simulate your design.

References

1) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010.
2) Perry, Douglas L, **VHDL,** New York : McGraw-Hill, c1991
3) Botros, Nazeih, HDL with digital design : VHDL and Verilog, Dulles, Virginia : Mercury Learning and Information, [2015]
4) Vahid, Frank, VHDL for digital design, Hoboken, N.J. : Wiley, c2007
5) Short, Kenneth L, VHDL for engineers, Upper Saddle River, NJ : Pearson Prentice Hall, c2009
6) Coelho, David R., The VHDL Handbook, Boston, MA : Springer US, 1989
7) Lipsett, Roger., VHDL: Hardware Description and Design, Boston, MA : Springer US, 1989