Student Name:

Student ID:

Date: 19/11/2021

Instructor: Mustafa Altun

EHB 205E: Introduction to Logic Design

MIDTERM I

Duration: 120 Minutes

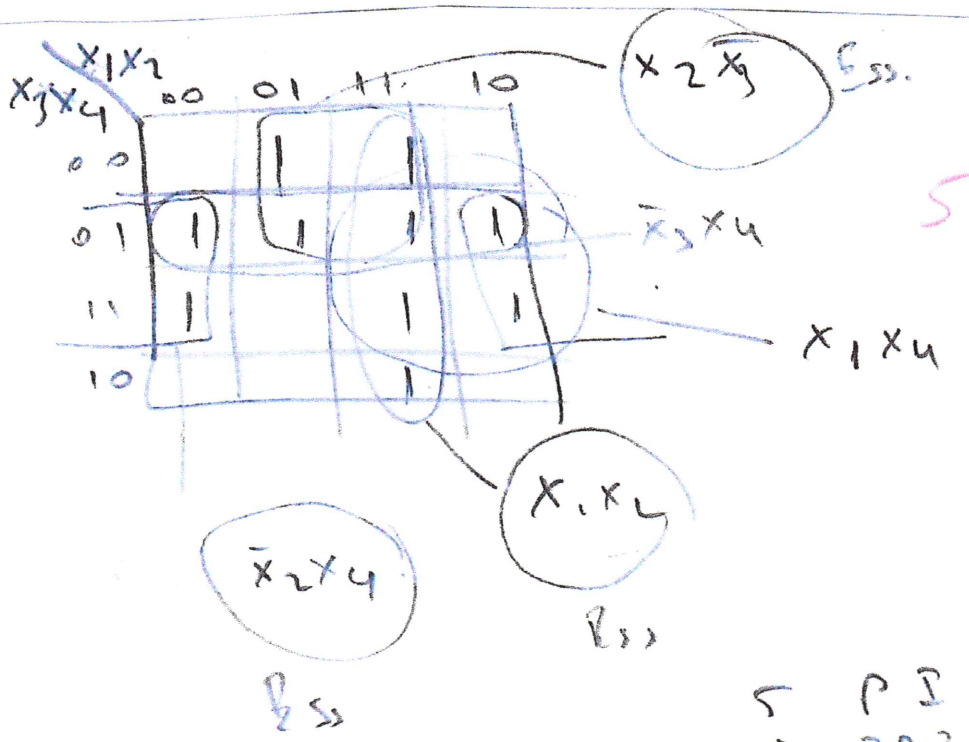
Grading: 1) 15%, 2) 30%, 3) 25%, 4) 30%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

GOOD LUCK!

1) Consider a 4-variable Boolean function $f(x_1, x_2, x_3, x_4) = \sum(1,3,4,5,9,11,12,13,14,15)$; x_1 is the most significant bit. Obtain a minimal sum-of-products (SOP) expression for f using a **Karnaugh** map. Show all prime and essential prime implicants.



5 PI's
3 EPI's

5

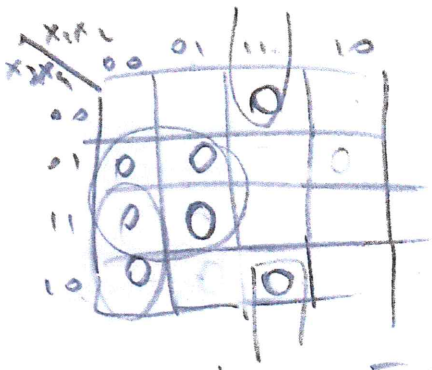
$$f = x_1x_2 + x_2\bar{x}_3 + \bar{x}_2x_4$$

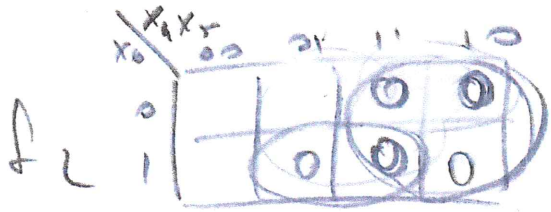
5

2) Consider a 6-variable Boolean function $f = f_1(x_1, x_2, x_3, x_4) \cdot f_2(x_4, x_5, x_6)$ where $f_1 = \prod(1,2,3,5,7,12,14)$ - x_1 is the most significant bit, and $f_2 = \prod(3,4,5,6,7)$ - x_4 is the most significant bit.

a) Obtain a minimal product-of-sum (POS) expression for f.

b) Implement f using only **two-input NAND** (NAND-2) gates; use minimal number of gates. Use only variables as inputs (**not their negated forms**).





f_1

f_2

$f_1 = (x_1 + \bar{x}_4)(\bar{x}_1 + \bar{x}_2 + x_4)(x_1 + x_2 + \bar{x}_3)$ 5

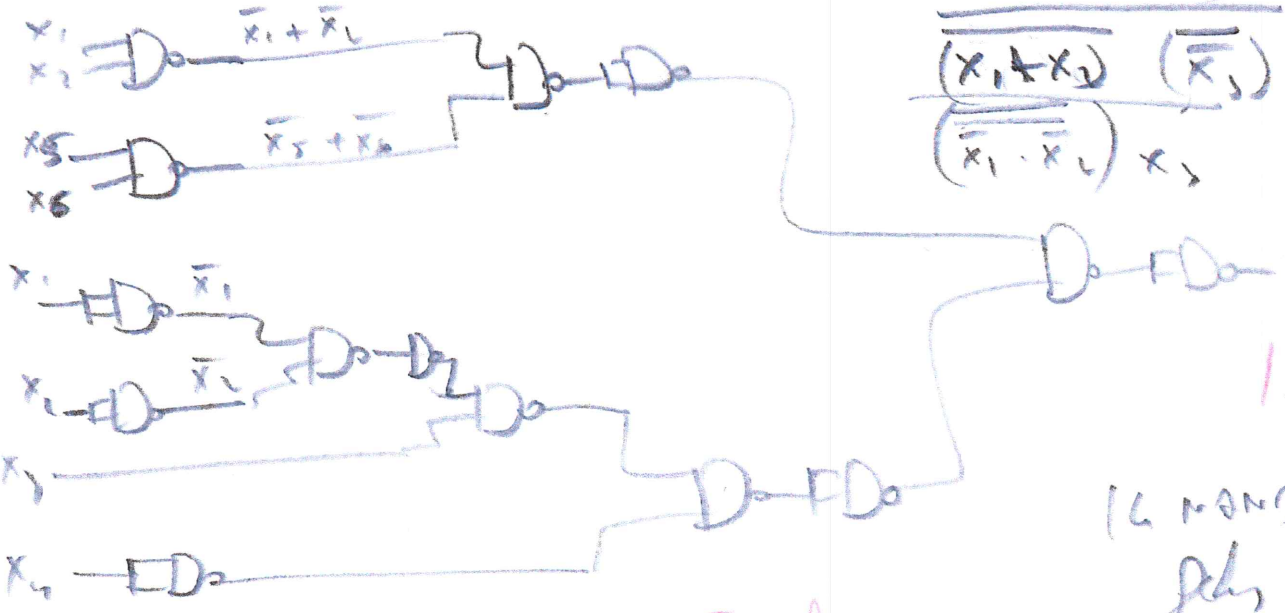
$f_2 = (\bar{x}_4)(\bar{x}_5 + \bar{x}_6)$ 5

$f = f_1 \cdot f_2 = (\bar{x}_4)(\bar{x}_5 + \bar{x}_6)(\bar{x}_1 + \bar{x}_2)(x_1 + x_2 + \bar{x}_3)$ 5

$\overline{(\overline{x_1 x_2})\,\overline{(x_5 x_6)}\,\overline{(\bar{x}_4)}\,\overline{(x_1 + x_2 + \bar{x}_3)}}$

$\overline{(x_1 + x_2)\,\overline{(\bar{x}_3)}}$

$(\bar{x}_1 \cdot \bar{x}_2)\, x_3$

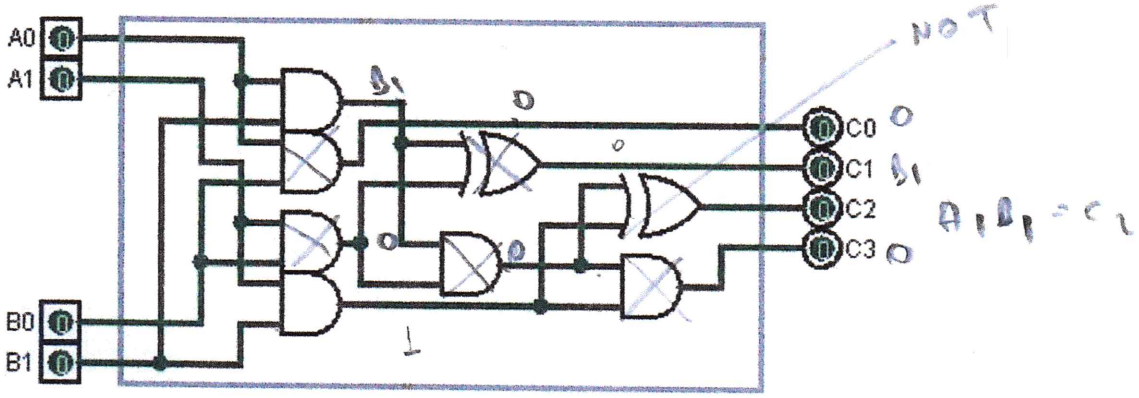


15

14 NAND gates

-1.5 for each added NAND

3) Consider a circuit consisting of AND-2 and XOR-2 gates with 4 inputs , **A0**, **A1**, **B0**, **B1**, and 4 outputs, **C0**, **C1**, **C2**, **C3**.



a) Derive truth table of this circuit.

b) Suppose that for a certain application, always **A0=1** and **B0=0**. For this scenario, simplify the circuit by only using NOR-2 gates.

a) $(A_1 A_0) \times (B_1 B_0) = C_3 C_2 C_1 C_0$ 15

b)

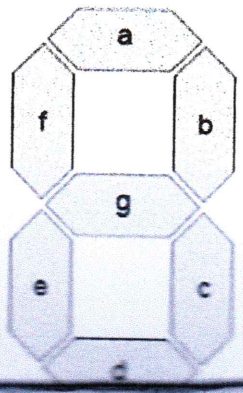
10

C_1 ——— D_1

0 ——— C_0

0 ——— C_3

4) Consider 4 binary inputs representing decimal numbers from 0 to 15. Also consider a 7-segment display as shown below. It only shows two letters: H (stands for high), and L (stands for low). If the decimal number is below 5, the display shows L; if the decimal number above 10 the display shows H; otherwise (5, 6, 7, 8, 9, 10) what the segment shows, does not matter Design a circuit consisting of minimal number of NAND-2 gates for this operation. Note that the circuit has 4 inputs and 7 outputs; 7 outputs of the circuit are connected to 7 segments **a**, **b**, **c**, **d**, **e**, **f**, and **g**. If a segment output is logic 1 then the corresponding segment is illuminated or lit.



	x_1	x_2	x_3	x_4	a	b	c	d	e	f	g
0	0	0	0	0				1	1	1	
1	0	0	0	1				1	1	1	
2	0	0	1	0				1	1	1	
3	0	0	1	1				1	1	1	
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1							
10	1	0	1	0							
11	1	0	1	1	1	1		1	1	1	
12	1	1	0	0	1	1		1	1	1	
13	1	1	0	1	1	1		1	1	1	
14	1	1	1	0	1	1		1	1	1	
15	1	1	1	1	1	1		1	1	1	

10

12 NAN

$b = c = g = x_1 x_2 + x_1 x_3 x_4$

$d = \bar{x}_1 \bar{x}_2 + \bar{x}_1 \bar{x}_3 \bar{x}_4$

$e = f = b + d$

$b = \overline{\overline{x_1 x_2} \cdot \overline{x_1 x_3 x_4}}$

$= \overline{\overline{x_1 x_2} \cdot \overline{(x_1 x_3)(x_4)}}$

$= \overline{\overline{x_1 x_2} \cdot (\overline{x_1 x_3})\, x_4}$ 5 NAN

10

$d \rightarrow 5 + 4 = 9$ NAND $\quad e \rightarrow 3$ N