ELE523E Computational Nanoelectronics, Fall 2018

Presentation Rules and Topics

RULES:

- Each student makes his/her presentation in **25** minute time span, **20** minutes for the presentation and **5** minutes for the questions/comments.
- Presentation topics and corresponding papers are listed below. The presentations should be mainly constructed on the listed papers; however it is encouraged to use/refer other papers and sources.
- Students should decide their presentation during the lecture time on **10/12/2018**.
- All students, not just the presenter, are expected to read the related papers before presentations. Students are expected to ask (tough☺) questions to the presenter.
- Students are graded considering the presentation **clarity/quality** and also the presenter's **knowledge** on the topic.

W14 (17/12/2018) TOPICS:

- **W14-P1, Reversible Computing:** Maslov, D., Dueck, G. W., & Miller, D. M. (2005). Toffoli network synthesis with templates. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, *24*(6), 807-817.
- **W14-P2, Reversible Computing:** Soeken, M., Wille, R., Hilken, C., Przigoda, N., & Drechsler, R. (2012, January). Synthesis of reversible circuits with minimal lines for large functions. In Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific (pp. 85-92). IEEE.
- **W14-P3, Reversible Computing:** Altun, M., Parvin, S., & Cilasun, M. H. (2018). Exploiting Reversible Computing for Latent-Fault-Free Error Detecting/Correcting CMOS Circuits. *IEEE Access*, accepted, 2018.
- **W14-P4, Molecular Computing:** Qian, L., & Winfree, E. (2011). Scaling up digital circuit computation with DNA strand displacement cascades. *Science*, 332(6034), 1196-1201.
- **W14-P5, Molecular Computing:** Cardelli, L. (2013). Two-domain DNA strand displacement. Mathematical Structures in Computer Science, 23(2), 247-271.
- **W14-P6, Nanoarray based Computing:** DeHon, A. (2003). Array-based architecture for FET-based, nanoscale electronics. *Nanotechnology, IEEE Transactions on*, *2*(1), 23-32.
- **W14-P7, Nanoarray based Computing:** Strukov, D. B., & Likharev, K. K. (2012). Reconfigurable nano-crossbar architectures. *Nanoelectronics, R. Waser, Eds*.

- **W14-P8, Nanoarray based Computing:** Tunali, O., Morgul, M. C., & Altun, M. (2018). Defect-Tolerant Logic Synthesis for Memristor Crossbars with Performance Evaluation. *IEEE Micro*, 38(5), 22-31.

W15 (24/12/2018) TOPICS:

- **W15-P1, Stochastic Computing:** Chen, H., & Han, J. (2010, May). Stochastic computational models for accurate reliability evaluation of logic circuits. In *Proceedings of the 20th symposium on Great lakes symposium on VLSI* (pp. 61-66). ACM.
- **W15-P2, Stochastic Computing:** Vahapoglu, E., & Altun, M. (2018). From Stochastic to Bit Stream Computing: Accurate Implementation of Arithmetic Circuits and Applications in Neural Networks. *arXiv preprint* arXiv:1805.06262.
- **W15-P3, Approximate Computing:** Han, J., & Orshansky, M. (2013, May). Approximate computing: An emerging paradigm for energy-efficient design. In Test Symposium (ETS), 2013 18th IEEE European (pp. 1-6). IEEE.
- **W15-P4, Approximate Computing:** Gupta, V., Mohapatra, D., Park, S. P., Raghunathan, A., & Roy, K. (2011, August). IMPACT: imprecise adders for low-power approximate computing. In Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design (pp. 409-414). IEEE Press.
- **W15-P5, Approximate Computing:** Venkatesan, R., Agarwal, A., Roy, K., & Raghunathan, A. (2011, November). MACACO: Modeling and analysis of circuits for approximate computing. In Proceedings of the International Conference on Computer-Aided Design (pp. 667-673). IEEE Press.
- **W15-P6, Fault Tolerance for Nanoarrays:** Hogg, T., & Snider, G. (2008). Defect-tolerant logic with nanoscale crossbar circuits. In *Emerging Nanotechnologies* (pp. 5-32). Springer US.
- **W15-P7, Fault Tolerance for Nanoarrays:** Tunali, O., & Altun, M. (2017). Permanent and transient fault tolerance for reconfigurable nano-crossbar arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 36(5), 747-760.
- **W15-P8, Fault Tolerance for Nanoarrays**: Peker, F., & Altun, M. (2018). A Fast Hill Climbing Algorithm for Defect and Variation Tolerant Logic Mapping of Nano-Crossbar Arrays. *IEEE Transactions on Multi-Scale Computing Systems*.