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# Design of positive feedback driven current-mode amplifiers Z-Copy CDBA and CDTA, and filter applications

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**Abstract** In this study, high-performance current-mode amplifiers Z-Copy current differencing buffered amplifier (ZC-CDBA) and current differencing trans-conductance amplifier (ZC-CDTA) are designed. In order to improve input impedances of the amplifiers, a new approach based on positive feedback is proposed. Impedance improvement/reduction is achieved by using only two extra transistors for each input. This number of extra transistors is very few compared to that in conventional negative feedback based improvement techniques. The proposed technique is justified by performing a detailed stability analysis. It is shown that the input impedances of ZC-CDBA and ZC-CDTA can be safely reduced to the level of 50 Ω by considering fabrication scatterings. The proposed amplifiers are verified with analog filter applications, a new KHN and recently proposed biquadratic and frequency agile filters. It is shown that the filters operate accurately at the frequency level of 100 MHz. This is a clear sign of the proposed amplifiers' high performance. Layout and post layout simulations are done for the proposed circuits using AMS 0.18 μm parameters in Cadence environment.

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**Keywords** Positive feedback · CMOS integrated circuits · Active filters · Current-mode circuits

## 1 Introduction

Current-mode analog circuits have been well investigated over the last decades as alterative of their voltage-mode counterparts. With the increasing importance of using low voltage supplies, current-mode circuits have recently attracted even more attention. Unlike conventional voltage-mode amplifiers whose DC swing performance is limited by voltage supplies, current-mode amplifiers can satisfactorily operate in low voltage values. Furthermore, current-mode amplifiers have significant advantages such as inherent wide bandwidth, wide dynamic range and simple circuitry with lover voltage supplies [16, 18]. In this study, we propose new current-mode circuit structures for "Z Copy Current Differencing Buffered Amplifier (ZC-CDBA)" and "Z Copy Current Differencing Trans-conductance Amplifier (ZC-CDTA)" that were recommended as versatile current mode analog building blocks by Biolek [11]. With an addition of the Z-Copy terminal, the universality of CDBA [1, 10] and CDTA [13, 17] was improved. A conventional current mirror or the third generation current conveyor can be used to achieve Z-Copy output current [12].

For the proposed amplifiers, we first focus on achieving low input impedance values that is very beneficial and necessary for current amplifiers. Current amplifiers ideally have zero input impedances. Indeed, input impedance values determine the minimum required resistance values in application circuits. For example, if a current amplifier, in filter application, has an input impedance of 5 kΩ then the resistor values of the filter should be chosen at least

50 kΩ for proper operation. This also affects the minimum required capacitor values of the filter. Considering that resistors and capacitors occupy most of the circuit (layout) area, low input impedance/resistance is essential for current amplifiers. In the literature, reducing the input resistance values is mostly achieved by using negative feedback with an additional amplifier [5, 6, 15]. This technique works properly at the cost of an extra amplifier that significantly increase the circuit area and worsens the amplifier's frequency response. In this study, we propose a new way of reducing input resistance values: using positive feedback. The reduction is achieved by using only two extra transistors for each input. Since the input stage of the amplifiers is a current differencing unit with two inputs P and N, total of four extra transistors are needed.

We design the output stage of the proposed ZC-CDBA as a voltage buffer. The amplifier has high impedance Z and Z-Copy terminals, and a low impedance W terminal. We design the output stage of the proposed ZC-CDTA as a floating current source. The amplifier has high impedance X−, X+, Z, and Z-Copy output terminals.

This paper is organized as follows. In the second section, the proposed reduction method for input impedance is introduced. Comparison of the method with conventional methods is presented. In third section, the CMOS implementations and layouts of ZC-CDBA and ZC-CDTA are given. The impedance characteristics of the current mode active blocks are shown at the beginning of this section. Additionally, the impedance values are justified by performing a detailed stability analysis. The stability and worst case analysis for the amplifier's input impedances are shown at the second part of this section. The other characteristics of ZC-CDBA and ZC-CDTA are also given in the same section. In the last section, two current mode filter applications are presented. The first proposed filter contains two ZC-CDBAs, two grounded capacitors, and one resistor. The second filter, frequency agile filter, contains ZC-CDTA and ECCII (electronically controllable second generation current conveyor). The performance of the filters is tested in this section. Sensitivity values of the filters are also given.

## 2 Reduction method for input impedance

In this section positive feedback technique for reducing input impedance is studied. The advantages of using positive feedback are formulized with circuit diagrams.

### 2.1 Positive feedback versus negative feedback

Reducing input resistance values is conventionally achieved by using negative feedback based methods. In this study, we propose a method based on positive feedback for this purpose. The proposed method with a comparison of the conventional one is analyzed in details.

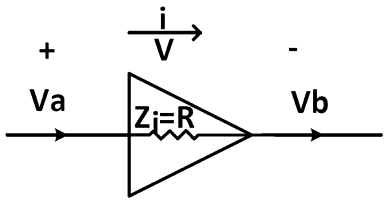


**Fig. 1** A system without feedback

Figure 1 shows a system without feedback. The internal impedance value of a general system is the ratio of the voltage over the system to the current which flows inside of the system according to Ohm's law. The internal impedance for Fig. 1 is given in Eq. 1. The internal impedance is equal to R for purely resistive circuits.

$$Z_i = \frac{V}{i} = \frac{V_b - V_a}{i} = R \tag{1}$$

Figure 2 shows the negative feedback system to reduce the input impedance. Equation 2 gives the internal impedance value for negative feedback system. In this equation, $\boldsymbol{AZ_i}$ represents the reduction factor; the larger the reduction factor the smaller the resistance values obtained. For example, if an amplifier has an input impedance of 10 kΩ and 100 Ω is required for a certain application then this reduction factor is approximately 100 (10 kΩ/100 Ω).

$$\frac{V}{i} = \left(\frac{1}{1 + AZ_i}\right) Z_i \tag{2}$$

Figure 3 shows the positive feedback system to reduce the input impedance. Equation 3 gives the internal impedance value for positive feedback system. In this equation, $\boldsymbol{AZ_i}$ represents the reduction factor; the closer the reduction factor to one the smaller the resistance values obtained. For example, if an amplifier has an input impedance of 10 kΩ and 100 Ω is required for a certain application then this reduction factor is approximately one (1–100 Ω/10 kΩ).

$$\frac{V}{i} = (1 - AZ_i) Z_i \tag{3}$$

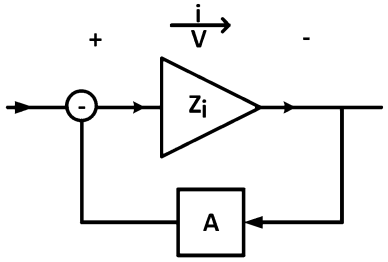


**Fig. 2** The negative feedback system; input is voltage

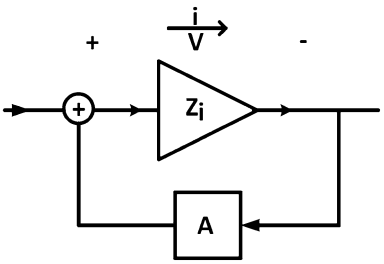


**Fig. 3** The positive feedback system; input is current

In order to achieve a certain reduction factor for negative feedback based method, an amplifier with a gain that equals to the reduction factor, should be added [9, 15]. For example, if a reduction factor of 100 is needed then an amplifier with a gain of 100 should be added to the original circuit. This is quite costly in terms of the number of added transistors. On the other hand, in order to achieve a certain reduction factor for positive feedback based method, an amplifier with a gain of approximately unity should be added. In this study this is achieved with using only two added transistors. The current differencing unit CMOS realization without any feedback system is given in Fig. 4. The added (extra) circuitries for negative feedback are given in Fig. 5. The proposed reduction method is shown in Fig. 6.

The basic differential pair used as an amplifier to provide negative feedback system is not enough to obtain lower impedance values compared with positive feedback technique. Two stages operational amplifier must be designed to achieve 50 Ω impedance levels. In this case, the CMOS realization of the current differencing unit has not only very large chip area but also has very complicated CMOS realization. Note that the negative feedback structure uses two extra amplifiers (eight transistors) compared to four extra transistors used in the positive feedback

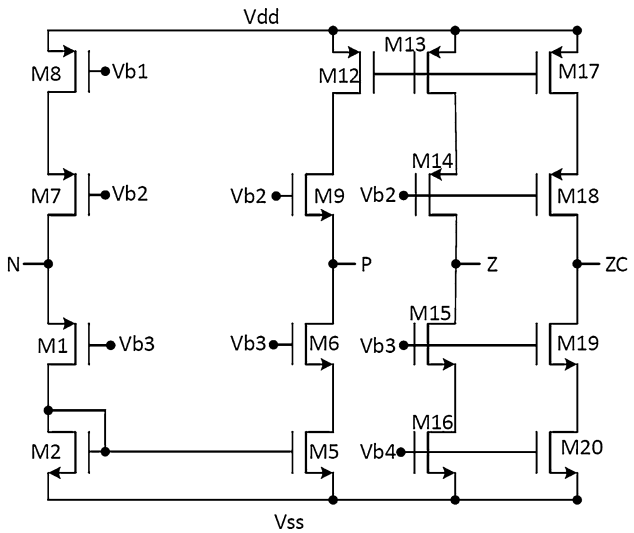


**Fig. 4** The current differencing CMOS realization without feedback

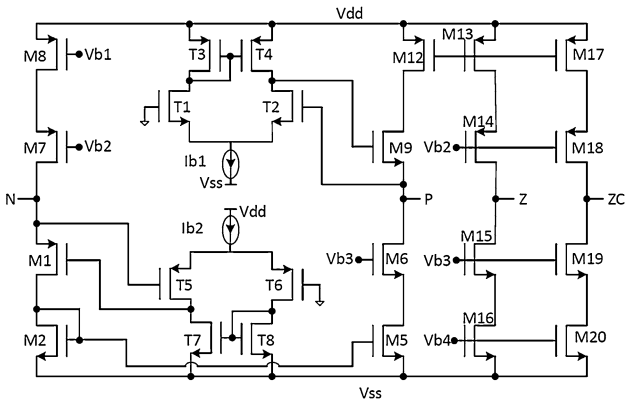


**Fig. 5** The current differencing CMOS realization with negative feedback

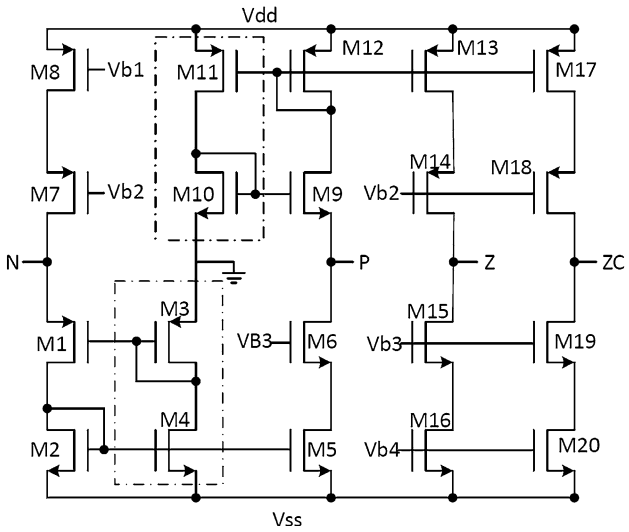


**Fig. 6** The current differencing CMOS realization with positive feedback

structure. The input impedance comparison for the current differencing CMOS realization without feedback, with positive feedback and negative feedback is given in Table 1. The values in the table are clearly in favor of using positive feedback. With positive feedback, nearly 10 times smaller resistance values are achieved compared to those with negative feedback.

The only disadvantage of using positive feedback can be the stability problem. For defeating this problem, a detailed stability analysis is performed in the next section, and it is shown that the input impedance values as low as 50 Ω can safely be implemented.

## 3 Current-mode amplifiers (ZC-CDBA and ZC-CDTA)

The block diagrams for ZC-CDTA and ZC-CDBA are given in Figs. 7 and 8, respectively.

**Table 1** The input impedance comparison

| | Without feedback (kΩ) | Negative feedback (Ω) | Positive feedback (Ω) |
|---|---|---|---|
| N terminal input impedance | 1.2 | 724 | 57 |
| P terminal input impedance | 1.3 | 653 | 44 |

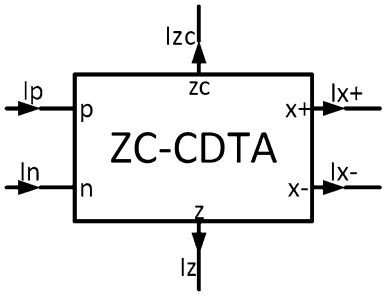


**Fig. 7** ZC-CDTA block diagram

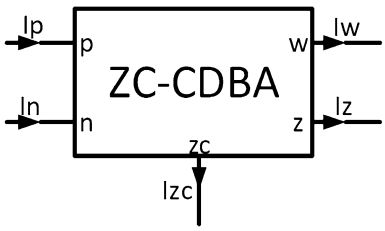


**Fig. 8** ZC-CDBA block diagram

ZC-CDTA has two input terminals and four output terminals. The input terminals are low impedance nodes. The output terminals are high impedance nodes. ZC-CDBA has two input terminals and three output terminals. The input terminals are low impedance nodes. Two of the output terminals (Z, Z Copy) are high impedance and the other (W) is low impedance nodes.

The proposed CMOS structure of the ZC-CDBA and ZC-CDTA are shown in Figs. 9 and 10, respectively. The equation matrix of the ZC-CDBA is given in Eq. 4. In Eq. 5 shows the equation matrix of ZC-CDTA.

$$\begin{pmatrix} i_z \\ i_{zc} \\ V_w \\ V_p \\ V_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_z \\ i_w \\ i_p \\ i_n \\ i_z \end{pmatrix} \tag{4}$$

$$\begin{pmatrix} V_p \\ V_n \\ i_z \\ i_x \\ i_{zc} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} i_p \\ i_n \\ V_x \\ V_z \\ i_z \end{pmatrix} \tag{5}$$

M1–M20 transistors of the ZC-CDBA and the ZC-CDTA belong to the current differencing unit, which has Z and Z copied output. M21–M28 transistors of the ZC-CDBA are the voltage buffer's transistors. M1–M4 transistors of the ZC-CDTA are the floating current source's transistors [8]. Transistor ratios of ZC-CDBA are shown in Table 2. Transistor ratios of ZC-CDTA are shown in Table 3.

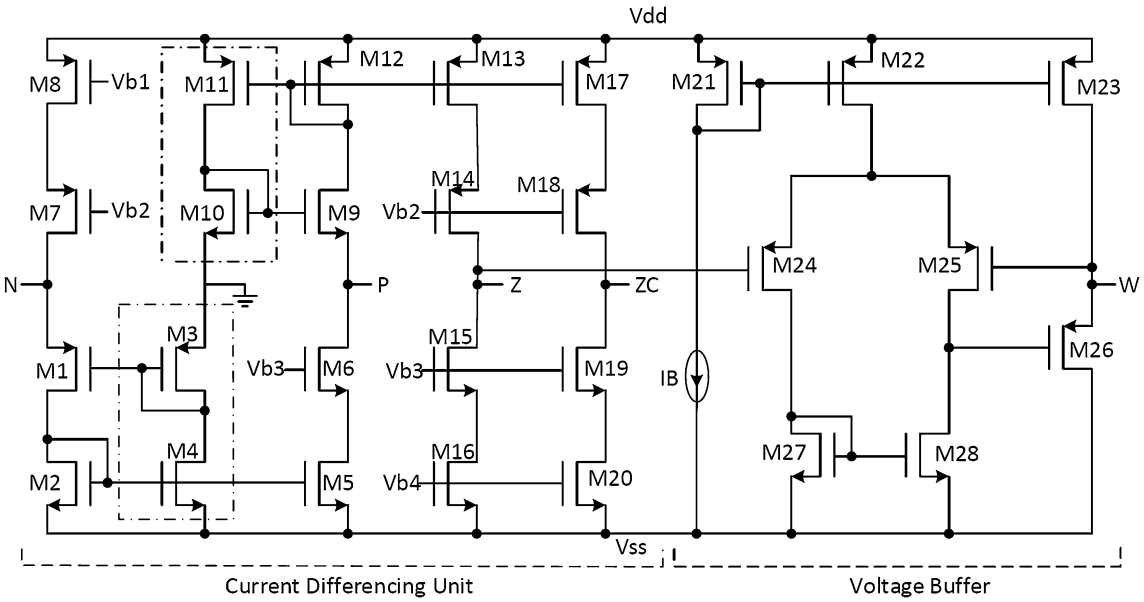


**Fig. 9** CMOS Realization of ZC-CDBA

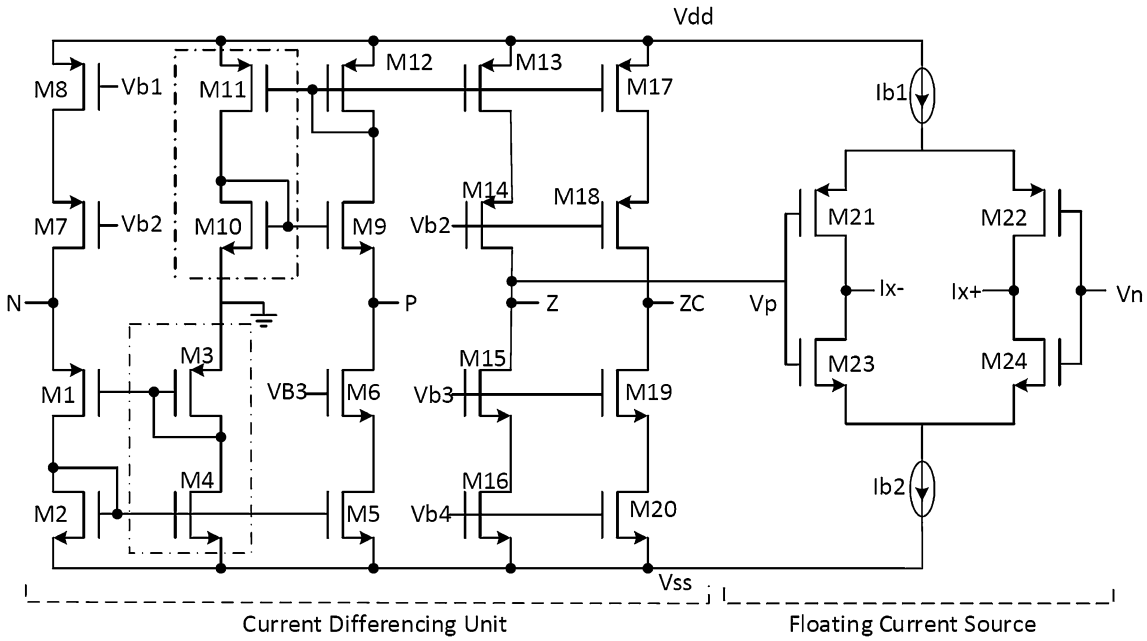


**Fig. 10** CMOS Realization of ZC-CDTA

**Table 2** Transistor ratios of ZC-CDBA

| Transistors | W (μm) | L (μm) |
|---|---|---|
| M1 | 12 | 0.36 |
| M2 | 120 | 0.36 |
| M3–M5 | 12 | 0.36 |
| M6–M9 | 12 | 0.36 |
| M10 | 120 | 0.36 |
| M11–M25 | 12 | 0.36 |
| M26 | 60 | 0.36 |
| M27–M28 | 12 | 0.36 |

**Table 3** Transistor ratios of ZC-CDTA

| Transistors | W (μm) | L (μm) |
|---|---|---|
| M1 | 12 | 0.36 |
| M2 | 120 | 0.36 |
| M3–M5 | 12 | 0.36 |
| M6–M9 | 12 | 0.36 |
| M10 | 120 | 0.36 |
| M11–M20 | 12 | 0.36 |
| M21–M24 | 1.44 | 0.36 |

The transistors used for positive feedback to reduce the P terminal input resistance are M10 and M11. The transistors used for positive feedback to reduce the N terminal input resistance are M3 and M4. The input terminal impedances formulas are given in Eqs. 6 and 7 [5, 6].

$$r_{in-} = \frac{1}{g_{m1}g_{m3}}\left\{(g_{ds1}+g_{m3}+g_{ds3}) - \frac{g_{m1}g_{m4}}{g_{ds4}+g_{m2}+g_{ds2}}\right\} \quad (6)$$

$$r_{in+} = \frac{1}{g_{m9}g_{m12}}\left\{(g_{ds9}+g_{m12}+g_{ds12}) - \frac{g_{m9}g_{m11}}{g_{ds11}+g_{m10}+g_{ds10}}\right\} \quad (7)$$

The layout of ZC-CDBA is given in Fig. 11. The size of the ZC-CDBA layout is 1070.19 μm$^2$. The layout of ZC-CDTA is given in Fig. 12. The size of the ZC-CDTA layout is 844.71 μm$^2$. All simulations are performed with the post-layout netlist.

### 3.1 Impedance characteristics of amplifiers

The input impedances of the P and N terminal are given in Figs. 13 and 14, respectively. The input impedance values are much smaller than those in [5, 6]. The biasing voltages; $V_{b1}$, $V_{b2}$, $V_{b3}$ and $V_{b4}$ voltages are selected as 500, −400, 100 and 300 mV, respectively. The $I_b$ current is selected as 30 μA.

The effect of the M3 and M4 transistors to the N terminal input impedance is given in Fig. 15. The effect of the M10 and M11 transistors to the P terminal input impedance is also given in Fig. 16.

The phase margin values show that, the real part of the impedance values are positive until 1 GHz frequency level for both P and N terminals. The desired input impedance level can be obtained by changing W/L ratios of these transistors.

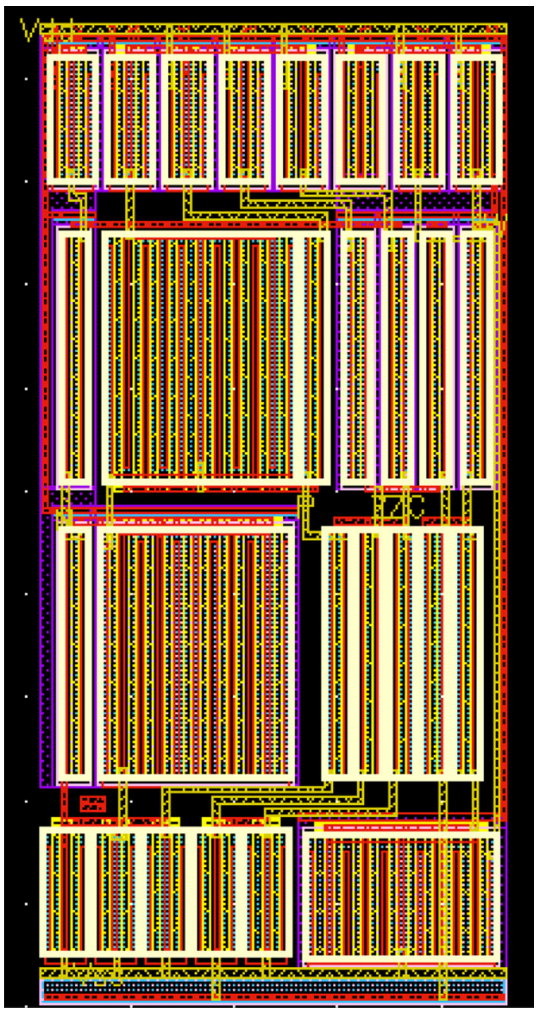

**Fig. 11** The layout of ZC-CDBA

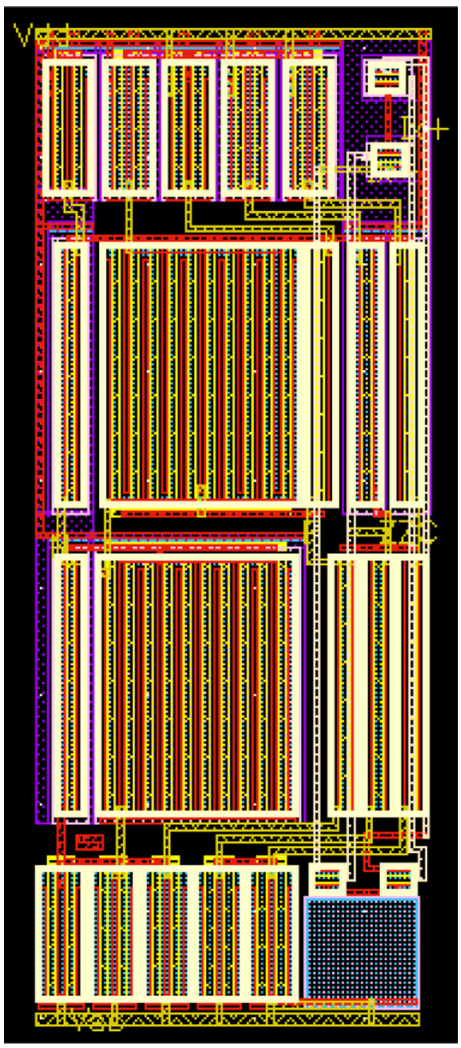

**Fig. 12** The layout of ZC-CDTA

It can be easily observed from Fig. 15, the input impedance is reduced by increasing the width of M3 and by decreasing the width of M4. From Fig. 16, the low input impedance is improved by increasing the width of M10 and by reducing the width of M11. From the figures, it can be derived that M4 and M11 transistors' width should be selected greater than 12 μm.

### 3.2 Stability and worst case analysis of amplifiers

Positive feedback is generally forbidden (except oscillator circuits) because of the stability problem. It is shown that, if used carefully, it is very effective for input impedance reduction.

The worst case analysis for Zn and Zp are given in Figs. 17 and 18, respectively. The corner analyses are done for the input impedances of designed circuits to check its behaviors under various conditions of temperature and scattering of supply voltages. The fabrication conditions

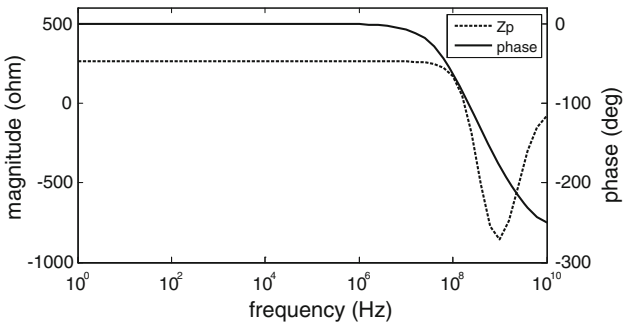


**Fig. 13** Input impedance characteristic of terminal-P

are selected with three parameters (ss, tt, ff). The temperature conditions are selected (−60 and 120°). The supply voltage conditions are selected (±1.1 and ±0.9 V).

The system is stable for all different conditions of worst case parameters. The input impedance levels are chosen

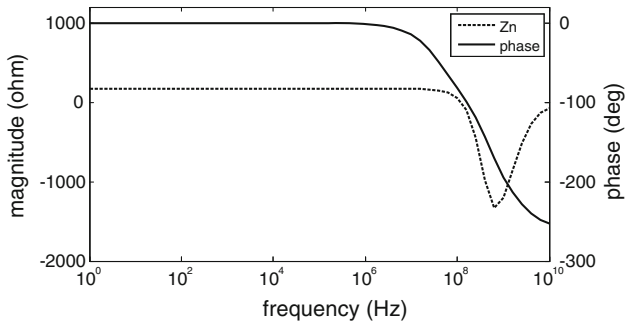


**Fig. 14** Input impedance characteristic of terminal-N

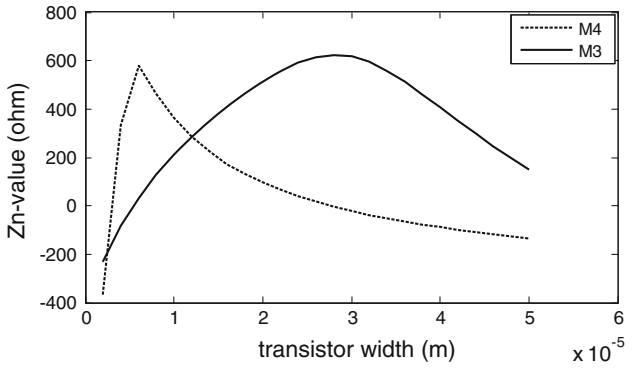


**Fig. 15** The effect of the M3 and M4 transistors' width to the N terminal input impedance

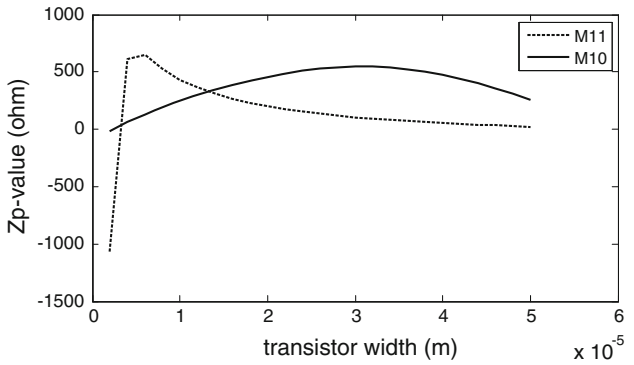


**Fig. 16** The effect of the M10 and M11 transistors' width to the P terminal input impedance

higher than the allowed minimum input impedance level to add more stability. For the proposed amplifiers, we select 263 and 164 Ω input resistance values according to the worst case analysis for temperature (−60 and 120 °C), supply voltage (±1.1 and ±0.9 V), and process variations (change in transistor dimensions). This is illustrated in Figs. 19 and 20. We also show that impedance levels as low as 45 Ω can be safely achieved by only considering process variations. This is illustrated in Figs. 21 and 22. All Monte Carlo analysis are performed for 200 samples.

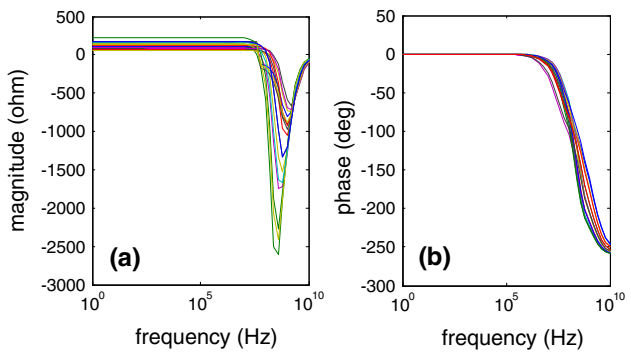


**Fig. 17** The impedance characteristics of terminal-N based on different corners **a** magnitude, **b** phase response

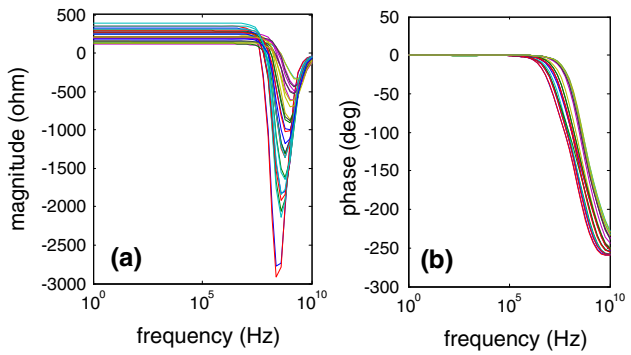


**Fig. 18** The impedance characteristics of terminal-P based on different corners **a** magnitude, **b** phase response

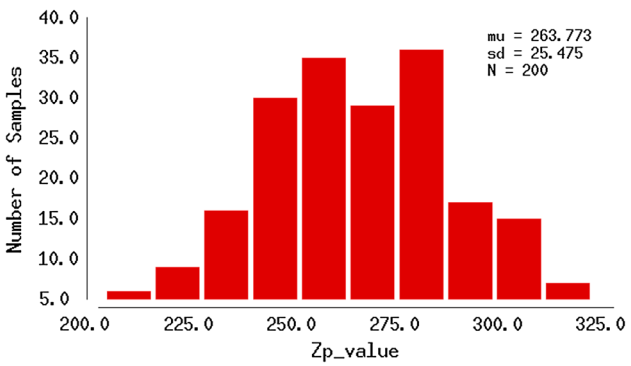


**Fig. 19** Monte Carlo analysis for Zp used in this study

### 3.3 Main characteristics of ZC-CDBA and ZC-CDTA

The Z terminal current characteristic for ZC-CDBA and ZC-CDTA is given in Fig. 23. The Z terminal current dynamic range is observed between −50 and 50 μA.

The voltage transfer characteristic of ZC-CDBA is given in Fig. 24. Z terminal output impedance for ZC-CDBA and ZC-CDTA are shown in Fig. 25. Figure 26 shows the W terminal output impedance of ZC-CDBA. ZC-CDBA's W

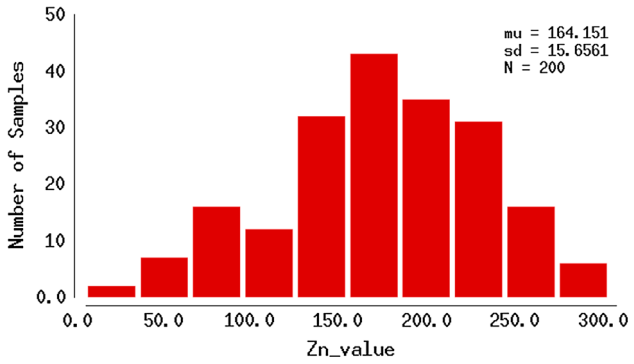


**Fig. 20** Monte Carlo analysis for Zn used in this study

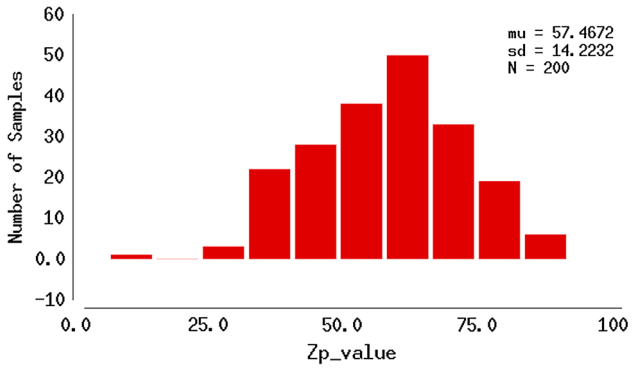


**Fig. 21** Monte Carlo analysis for minimum achievable Zp

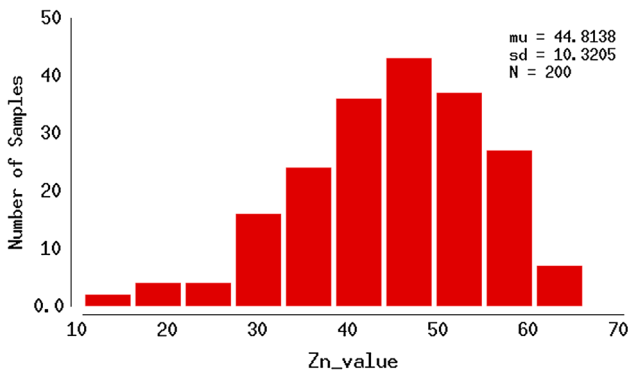


**Fig. 22** Monte Carlo analysis for minimum achievable Zn

terminal voltage dynamic range is observed between 215 and −215 mV.

The output impedance at Z terminal is found as 243 kΩ. The Z terminal output impedance value is enough to drive the load of the proposed applications. The W terminal output impedance is found as 215 Ω.

The summary of the simulation results of the proposed ZC-CDBA is given in Table 4. Some performance parameters are also given for ZC-CDTA in Table 5.

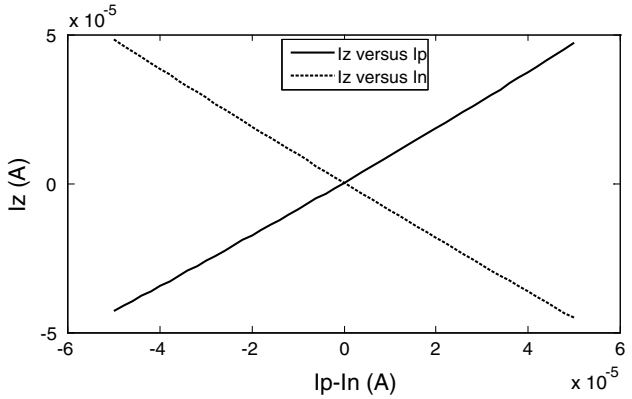


**Fig. 23** The characteristic of Z terminal current versus to the P and N terminal currents

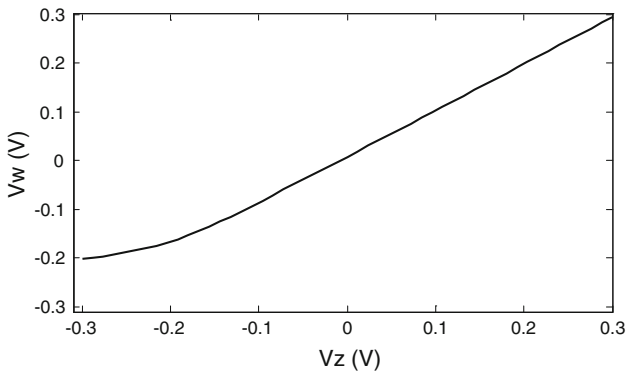


**Fig. 24** The characteristic of output terminal-W voltage versus to Z terminal voltage for ZC-CDBA

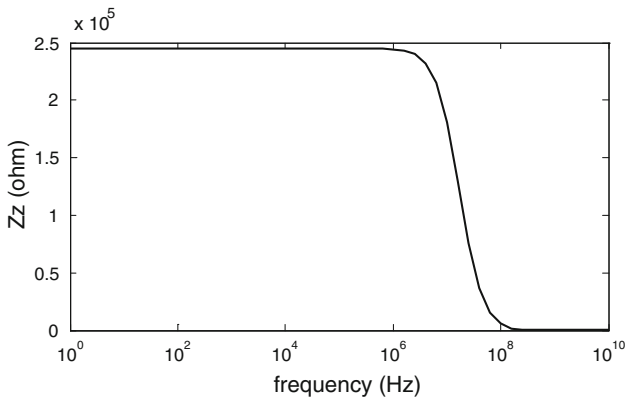


**Fig. 25** The Z terminal output impedance

Note that $f_{-3dB}$ frequency for $I_z/I_n$ and $I_z/I_p$ are appropriate for the application circuits up to 150 MHz cut-off frequency levels. The ZC-CDTA's X output terminals impedance level is observed as 257 kΩ. This impedance level is also suitable for the proposed design examples.

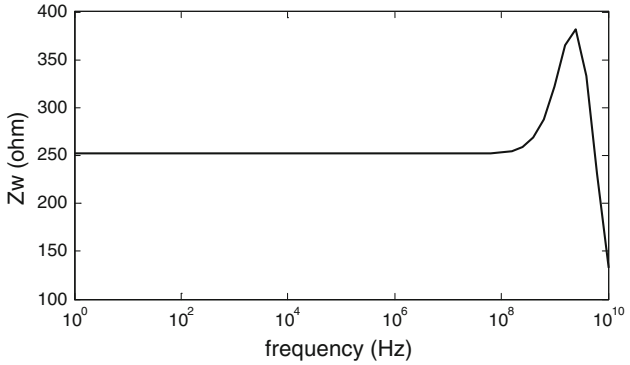


**Fig. 26** The W terminal output impedance

**Table 4** Performance of ZC-CDBA

| Results | Values |
|---|---|
| Supply voltage | ±1 V |
| Z terminal current dynamic range | −50 μA ≤ Iz ≤ 50 μA |
| W terminal voltage dynamic range | −215 mV ≤ Vw ≤ 215 mV |
| $f_{-3dB}$ frequency for Iz/In | 174.651 MHz |
| $f_{-3dB}$ frequency for Iz/Ip | 238.849 MHz |
| P terminal input impedance | 263.773 Ω |
| N terminal input impedance | 164.151 Ω |
| Current gain ($I_z/I_{p,n}$) | 1.015 |
| Voltage gain ($V_w/V_z$) | 0.996 |
| W terminal output impedance | 214.674 Ω |
| Z terminal output impedance | 242.677 kΩ |
| $f_{-3dB}$ frequency for Vw/Vz | 243.432 MHz |
| Power consumption | 1.58 mW |

**Table 5** Performance of ZC-CDTA

| Results | Values |
|---|---|
| Supply voltage | ±1 V |
| Power dissipation | 1.08 mW |
| Z terminal current dynamic range | −50 μA ≤ Iz ≤ 50 μA |
| $f_{-3dB}$ frequency for Iz/In | 174.651 MHz |
| $f_{-3dB}$ frequency for Iz/Ip | 238.849 MHz |
| P terminal input impedance | 263.773 Ω |
| N terminal input impedance | 164.151 Ω |
| Current gain ($I_z/I_{p,n}$) | 1.015 |
| Z terminal output impedance | 242.677 kΩ |
| $g_m$ (trans-conductance gain) | 51.773 μS |
| X− terminal output impedance | 256.480 kΩ |
| X+ terminal output impedance | 256.480 kΩ |

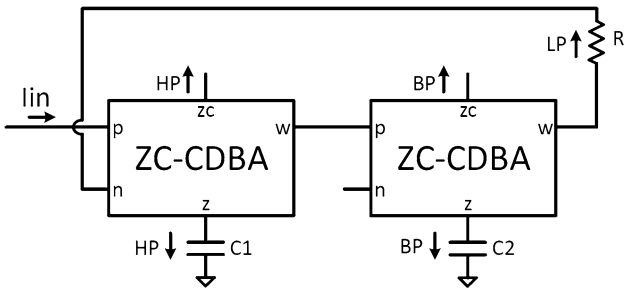


**Fig. 27** ZC-CDBA filter application

## 4 Design example

### 4.1 KHN filter based on ZC-CDBA

KHN filter structure is one of the widely used filter structures in analog signal processing. KHN filter was proposed by Kerwin, Huelsman, and Newcomb using state-variable synthesis in 1967. It has also been produced commercially.

The most important characteristic of the KHN filter transfer function is the adequacy for different type of filter implementation (band pass, high pass, low pass) at the same time. Another important property of KHN filter is the conformity for low sensitivity realization.

The proposed application circuit employing two ZC-CDBAs and three passive elements is given in Fig. 27. The proposed filter is the developed version those in [4]. The circuit of the KHN filter has two band pass filter sections, two high pass filter sections and one low pass filter section. One of the high pass filter sections has high impedance. The grounded capacitors $C_1$ and $C_2$ are selected as 200 fF. The resistor value is selected as $R = 800\ \Omega$. The capacitors and resistor values are selected to provide 100 MHz center frequency. The performance of the current differencing unit with positive feedback is verified with KHN filter.

The routine node analyses of the proposed topology yield the following transfer functions for high-pass, band-pass, low-pass filter given in Eqs. 8, 9 and 10, respectively. The pole angular frequency $\omega_0$ and the quality factor $Q$ are given in Eq. 11.

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2}{s^2 + s\frac{1}{C_1} + \frac{G}{C_1C_2}} \tag{8}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{s\frac{1}{C_1}}{s^2 + s\frac{1}{C_1} + \frac{G}{C_1C_2}} \tag{9}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\frac{G}{C_1C_2}}{s^2 + s\frac{1}{C_1} + \frac{G}{C_1C_2}} \tag{10}$$

$$\omega_0 = \sqrt{\frac{G}{C_1 C_2}}, \quad Q = \sqrt{\frac{GC_1}{C_2}} \tag{11}$$

Sensitivity analyses of the proposed filter with respect to active and passive components yield the following Eqs. 12 and 13, respectively.

$$S_G^{W_0} = -S_{C_1}^{W_0} = -S_{C_2}^{W_0} = 0.5 \tag{12}$$

$$S_G^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = 0.5 \tag{13}$$

The sensitivity values are satisfactorily very small. Therefore, the proposed filter configuration enjoys low sensitivity performance. To obtain filter characteristics, layout and post-layout simulations are done for proposed circuits.

The post-layout simulated responses of low-pass, band-pass, high-pass filters are given in Fig. 28. The post-layout simulations are in a good agreement with the schematic versions. The KHN filter can operate up to 100 MHz.

### 4.2 An electronically controllable filter using ZC-CDTA

A special radio communication system known as software-defined radio (SDR) are performed by means of software on a personal computer or embedded system in contrast to typical hardware components (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.). SDR characteristics as frequency, band-widths, modulation, etc. can be controllable and used as "computer tools" (software, RAM programmed, etc.). Also, cognitive radio is a different version of the software defined radio [14].

It is compulsory to catch different frequency by using designed hardware systems for some applications. For example, it is inevitable to implement the different positioning system protocols (GPS, GLONASS, Beidou, GNSS and Galileo) in the same chip. A reconfigurable receiver can be adapted different frequency [8].

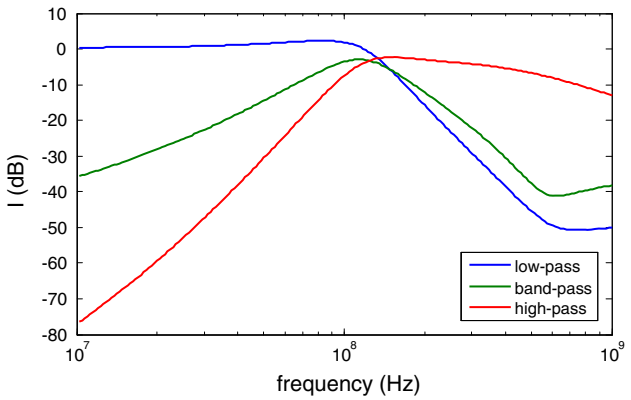


**Fig. 28** The gain-frequency responses of the proposed KHN filter

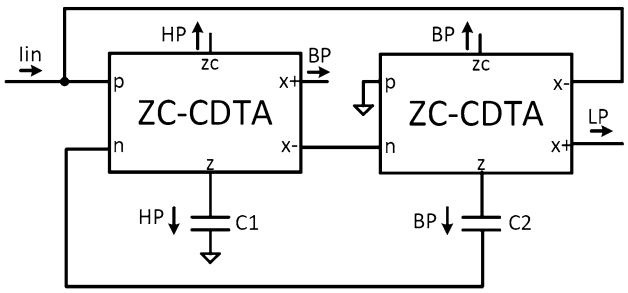


**Fig. 29** ZC-CDTA biquadratic filter structure [3]

The Z copied current differencing trans-conductance amplifier biquadratic filter structure is given in Fig. 29. The high-pass filter transfer function, band-pass filter transfer function, low-pass filter transfer function, the pole angular frequency $\omega_0$ and the quality factor Q are given in Eqs. 14, 15, 16, 17 and 18, respectively.

$$\frac{I_{HP}}{I_{IN}} = \frac{C_1 C_2 s^2}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{14}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{C_2 g_{m1} s}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{15}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{g_{m1} g_{m2}}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{16}$$

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{17}$$

$$Q = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}} \tag{18}$$

The sensitivities with respect to active and passive components are not larger than absolute value of 0.5.

The post-layout simulations for the biquadratic filter structure are shown in Fig. 30.

The basic biquadratic filter structure is modified by using electronically controllable second generation current

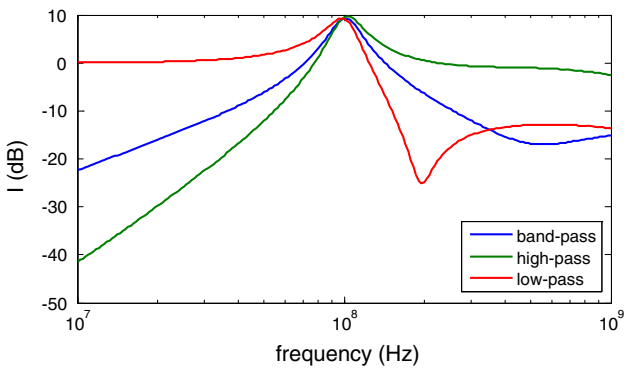


**Fig. 30** The gain-frequency responses of the biquadratic filter output

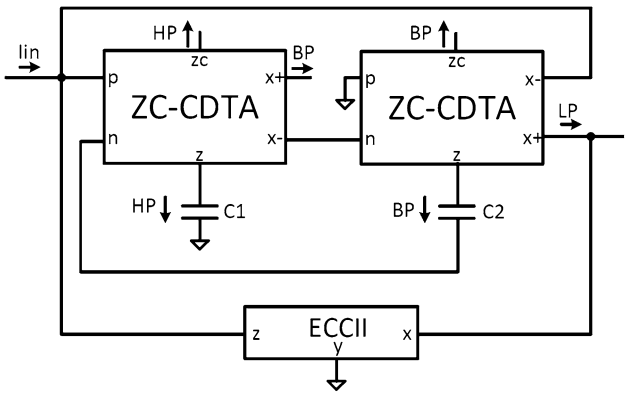


**Fig. 31** The electronically controllable filter using ZC-CDTA [2]

conveyor to obtain reconfigurable filter structure. The improved filter structure is shown in Fig. 31. The new band pass function of the filter is given in Eq. 19.

$$\frac{I_{BP}}{I_E} = \frac{\frac{C_2 g_{m1} s}{(1-A g_{m1} g_{m2})}}{1 + \frac{C_2 g_{m1} s}{(1-A g_{m1} g_{m2})} + \frac{C_1 C_2 s^2}{(1-A g_{m1} g_{m2})}} \tag{19}$$

The gain at $f_0$ of the band pass output does not change as before GBP = 1. The center frequency and the quality factor of the new filter structure are given in Eqs. 20 and 21, respectively.

$$\omega_0 = \frac{(1 - A g_{m1} g_{m2})}{2\pi\sqrt{C_1 C_2}} \tag{20}$$

$$Q = \sqrt{(1 - A g_{m1} g_{m2})}\frac{\sqrt{C_1 C_2}}{C_2 g_{m1}} \tag{21}$$

The quality factor and the center frequency of the controllable filter can be adjusted by the aid of current ratio (A) of the electronically controllable second generation current conveyor given in Fig. 31. The capacitance values are selected as C1 = C2 = 200 fF. The CMOS structure and the performance parameters of the ECCII are chosen as the same values those in [2]. In this work the performance of the current differencing unit with positive feedback is tested with reconfigurable filter structure.

The capacitance values are selected according to the suitable frequency range for positioning systems protocols (GPS, GLONASS, Beidou, GNSS and Galileo). The center frequency of band pass filter 88, 96, 102 and 108 MHz are obtained for bias current $I_A$ = 22, 16, 10 and 5 μA respectively. The $I_C$, $I_B$ bias currents of ECCII are selected as 60 μA.

Figure 32 shows the band pass output for different current ratio of the electronically controllable second generation current conveyor. The agile filter output is also appropriate for FM frequency range for receiver applications. The operating frequency of the biquadratic and frequency agile filter is improved up to 100 MHz compared those in [2, 3].

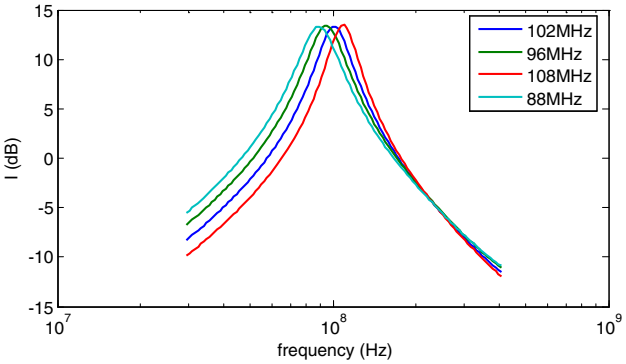


**Fig. 32** The reconfigurable filter output

## 5 Conclusion

The conventional wisdom is that analog circuits should not include positive feedback loops. As controversial as it seems, positive feedback is successfully used for impedance improvement in this study. With adding few transistors very low input resistance values are achieved for current amplifiers. Stability analysis is also performed and it is shown that input resistance values as low as 50 Ω can safely be implemented.

The proposed amplifiers ZC-CDBA and ZC-CDTA are simulated using post-layout parameters in Cadence environment. The size of the ZC-CDBA layout is 1070.19 $\mu m^2$; the size of the ZC-CDTA layout is 844.71 $\mu m^2$. AMS 0.18 μm transistor parameters are used in the simulations.

The proposed current amplifiers are also tested in filter applications. A new KHN and electronically controllable filter configurations are proposed. The total harmonic distortion of the KHN and frequency agile filters are measured with applied 100 μA sine wave at 100 MHz. The distortions are smaller than 5 %. It is shown that the filters operate accurately to the frequency level of 100 MHz. These are the clear signs of the proposed amplifiers' high performance.

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