Spin-Torque Memristor based Offset Cancellation Technique for Sense Amplifiers

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***Abstract*—In this study, we propose an offset cancellation technique with the spin-torque memristors where are unpredictable threshold voltage changes of transistors that results in the input referred random offset (IRRO) of amplifiers. Motivated by this fact, this study focuses on the IRRO cancellation in sense amplifiers with the aid of the spin-torque memristor technology. The spin-torque memristors in series perform less resistance and process variations from parallel connection. The resistance value of the spin-torque memristor was regarded as frozen when the current flow over the spin-torque memristor is lower than its critical switching current value. In fact, the proposed structure employs a non-destructive sensing scheme in order to achieve a relatively large sense margin by reducing the IRRO. Our main idea is to reduce or eliminate the IRRO exploiting the spin-torque memristors for providing the current matching on the input transistors of the voltage comparator. In particular, the overwrite problem of the spin-torque memristor was solved by setting the critical switching current of the spin-torque memristor to be greater than a current value corresponding to maximum the IRRO value. We evaluated the IRRO cancellation technique on the proposed comparator or sense amplifier using 45nm predictive CMOS technology. Although sense amplifiers are targeted in this study, our technique can be applied to any analog amplifier suffering from the IRRO.**

I. Introduction

Spin-torque memristor [1] is a promising technology for the implementation of memories thanks to its unlimited endurance, nonvolatility, and zero standby leakage power [2], while memristors have low switching speed and limited endurance [3]. The spin-torque memristor arrays with multi-cell structures have been successfully fabricated [4]. Although memory arrays have been fabricated with the spin-torque memristor technology, CMOS technology is still needed for the implementation of high performance sense amplifiers for memory arrays. However, with the continual diminishing of CMOS transistor sizes currently reaching a 10nm scale, the number of random dopant atoms in a transistor channel significantly decreases [5], [6]. This causes unpredictable threshold voltage changes of transistors that results in relatively high the input referred random offset (IRRO) of amplifiers [7]. Motivated by this fact, this study focuses on the IRRO cancellation in sense amplifiers with the aid of the spin-torque memristor technology.

Different topologies and methods for the IRRO, have been studied in the literature. These methods are classified as analog [8] and digital trimming [9]. However, these studies have common shortcomings; the resulting circuits suffer from large complexity, high power consumption, and relatively large area. In addition, the technique of laser trimming on sheet resistances can suffer from relatively high cost; they are only appropriate for high precision design [10]. More widely, the eliminating methods of the IRRO are studied in [11] that are mostly based on the switched capacitor architectures. Our technique has certain advantages considering these mentioned problems.

The proposed structure consists of the conventional voltage comparator and combination of the spin-torque memristors, where are connected between the source terminals of the input transistors of the voltage comparator. Similarly in [12], we proposed a digital trimming without using switched capacitors. Thus, we do not need multiple clock generation and distribution circuity entailing high power consumption. We used the negative pulse voltages switching from high resistance state to low resistance state because of more easily switching than other case. As a matter of fact, the resistance value of the spin-torque memristor was regarded as frozen; The current flow over the spin-torque memristor is lower than its critical switching current value. In fact, the proposed structure employs in a sense amplifier has a voltage driven nondestructive self-reference sensing scheme in order to achieve a relatively large sense margin by reducing the IRRO [13]

This paper is organized as follows. In Section II, we elaborate on the spin-torque memristor device properties and models supported by simulation results. In Section III, we present our offset cancellation technique with simulation results using 45nm predictive CMOS technology. Section IV concludes the paper.

II. Device Perspective

The magnetizations of a free layer (FL) and a pinned layer (PL) in the spin-torque memristor is widely studied with either perpendicular magnetic anisotropy (PMA) or in-plane magnetic anisotropy(IMA) [14], [15]. In this study, we decided to use a PMA-the spin-torque memristor device since PMA has a lower switching current than that of the IMA [5]. This operation allows us to achieve low power operation with the

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IRRO. The physical structure of the spin-torque memristor is represented in Fig. 1(a). It consists of the FL and the PL, that are separated from each other via a thin tunnel barrier (M_gO or AlO_x) the thickness of which determines the resistance of the spin-torque memristor. Furthermore, both thickness and material types of the FL determine the value of the threshold current of the spin-torque memristor. The layout of the spin-torque memristor is generated with back-end-of-the-line (BEOL) compatibility [16], as illustrated in Fig. 1(b). The equivalent circuit of the spin-torque memristor is represented as a variable resistor in Fig. 1(c). The spin-torque memristor has two different threshold currents, I_{C0+} and I_{C0-}, which are correspond to two different electrical resistance in according to the parallel (P) or anti-parallel (AP) magnetization configurations of the FL. These resistance values are the low resistance state (R_P) with positive currents and the high resistance state (R_{AP}) with negative currents. The magnetization dynamics

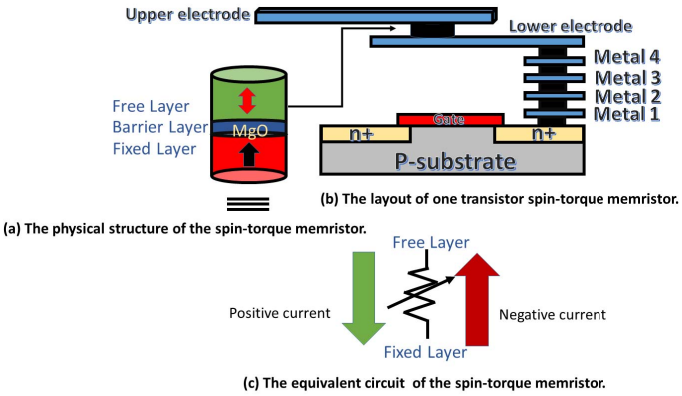

Fig. 1. (a) The spin-torque memristor physical structure, (b) The layout of the spin-torque memristor with a transistor, and (c) The equivalent resistance values of the spin-torque memristor.

of the FL in the spin-torque memristor are analyzed with Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation [15]. The average current density values, J_{CO}, change positively with the barrier height (E_B) values (20, 40, 60, 80), and negatively with pulse width (t_{pw}) values (0.2ns, 1ns, 10ns, 100ns). So in our simulations, these values were determined E_B=60, t_{pw}= 10ns. The average current density decreases when E_B values increase and the switching current probability density (from the high resistance state to the low resitance state) decreases when t_{pw} values decrease, as given in Fig. 2(a) and 2(b). Our simulation model, given in [17], is developed for solving the LLGS equation to catch dynamics of the spin-torque memristor by considering its physical parameters [14], [18].

The spin-torque memristor devices since it works as a unit of storage. The read and the write operations are two basic functions of the spin-torque memristor. In the read operation determines the bit value, and is significantly affected by the magnetoresitance ratio (MR), and its formula is MR=$\frac{(R_{AP}-R_P)}{R_P}$ [19]. The write operation is operated different switching mechanisms, such as the STT [15]. The writing cir-

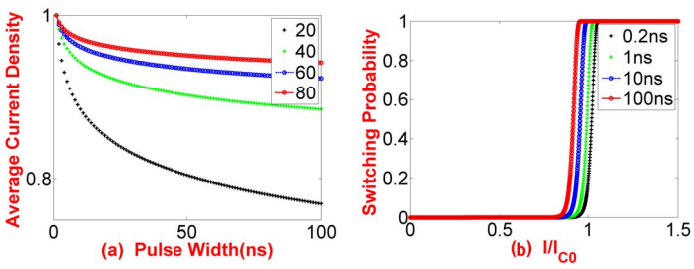

Fig. 2. (a) The average current density versus the pulse width, and (b) The switching current probability density versus normalized switching current.

cuitry of the spin-torque memristor, with its writing algorithm, and its incremental resistance flow are shown in Fig. 3 (a), (b), and (c), respectively. The resistance value of the spin-torque memristor changes with angle (θ) is given Eg. 1. On the other hand, the resistance variation (oxide thickness, t_{ox}, etc.) of the spin-torque memristor is assumed as 2.5 % in [20].

$$R(\theta) = (\frac{1}{R_P}(cos(\frac{\theta}{2}))^2 + \frac{1}{R_{AP}}(sin(\frac{\theta}{2}))^2)^{-1} \quad (1)$$

We achieved the different resistance values of the spin-torque memristor array by applying different voltage pulse amplitudes (range from -100mV to -500mV) to bit line (BL) assuming that the IRRO values in CMOS comparators are between 5mV and 50mV [10]. The resistance values of the spin-torque memristor in different device sizes with the same applied voltage pulses are shown in Fig. 4. To emphasize, the resistance of the spin-torque memristor varies with both the different voltage pulse widths, as well as the amplitudes and also the different sizes.

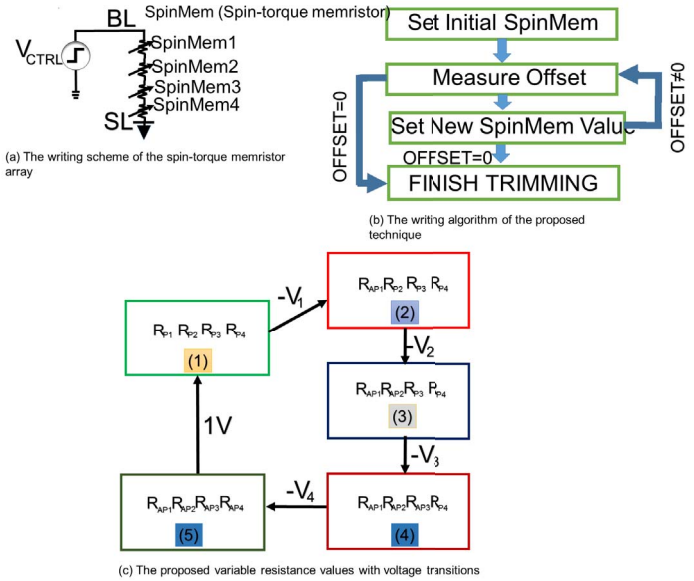

Fig. 3. The write operation of the spin-torque memristor.

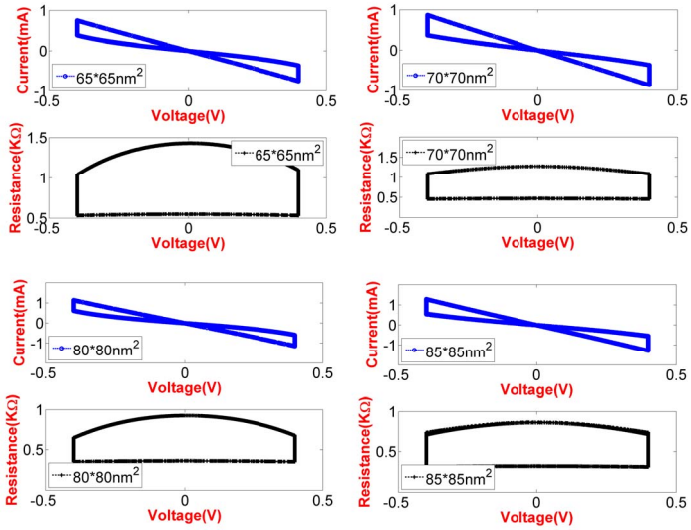

Fig. 4. The resistance values of the spin-torque memristor versus applied pulse voltages for the spin-torque memristor in different device sizes.

III. The IRRO for the Proposed Voltage Comparator

A conventional voltage comparator [21] is given in Fig. 5(a). It consists of a pre-amplifier stage, a decision stage, and an output buffer stage. The pre-amplifier is divided into three parts: the first is the diode connected PMOS loads (M_{P1} and M_{P2}), the second is the input transistors (M_{N1} and M_{N2}), and the third is the transistor current source loads (M_{NB} and M_{NB}).

To measure the IRRO, the negative input of the pre-amplifier was set to $V_{CM} = 0.5V$ (V_{DD}=1V), and the positive input of the pre-amplifier was changed from 0.35V to 0.55V. The switches ,V_{SW1} and V_{SW2} (with same pulse voltage amplitude and phase), are used to provide isolation between the proposed structure and the remaining part of the voltage comparator. On programming phase (the switches are OFF); firstly, the resistance values of the spin-torque memristors were initially programmed to high resistance state, and then these resistance values changed incrementally for wanted resistance values while applying the negative voltage pulses to the BL and in the same time, the source line (SL) is kept grounded, as illustrated in Fig. 5(b). Our main idea is to eliminate the IRRO exploiting the spin-torque memristors for providing the same current value for M_{N1} and M_{N2}. The minimum value of the IRRO occurs while X and Y nodes are shorted. However, considering the mismatch of M_{N1} and M_{N2} on physical design phase, the IRRO value in according to the short connection slides to a higher IRRO value. In this case, our proposed structure is intended to reduce this unexpected IRRO value. On evaluation phase, the proposed structure can be connected in either between Z and W nodes (Z-W) or between X and Y nodes (X-Y). Firstly, the IRRO cancellation results for Z-W were given in Fig. 6(a), but the obtained resistance values are not effective for the IRRO cancellation because the resistance values of the spin-torque memristor are less than the output resistance of pre-amplifier stage. Secondly, The IRRO cancellation results for X-Y were given in Fig. 6(b) in according to the four spin-torque memristor in series (R_0= between X and Y nodes are shorted, R_1=$R_{AP}, R_{AP}, R_{AP}, R_{AP}$, R_2=$R_P, R_{AP}, R_{AP}, R_{AP}$, R_3=R_P, R_P, R_{AP}, R_{AP}, R_4=R_P, R_P, R_P, R_{AP}, R_5=R_P, R_P, R_P, R_P), for the proposed resistance values of the spin-torque memristor assuming that both all of them are initially R_{AP} and the IRRO value is 20 mV.

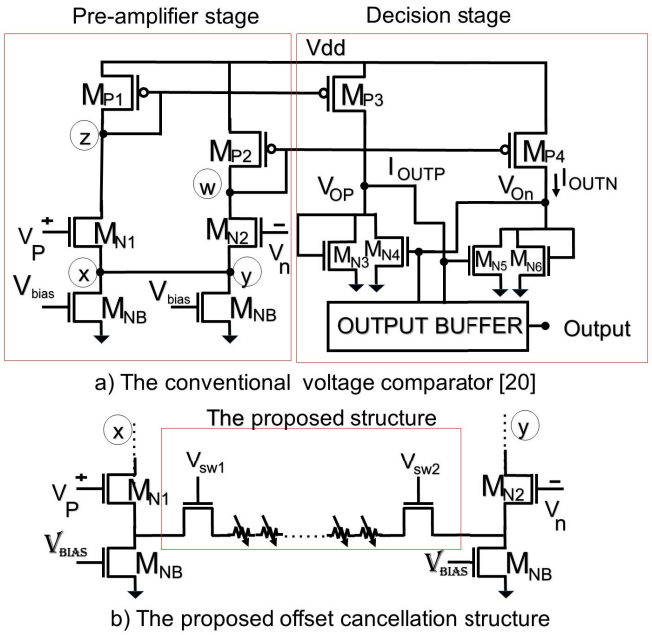

Fig. 5. (a) The conventional voltage comparator [21], and (b) The proposed IRRO cancellation technique.

A sense amplifier senses the data in the read operation. Also, a sense amplifier compares reference data against stored data. Importantly, the sense margin of a sense amplifier must be wider to prevent false reading data from memory cell. As a part of a sense amplifier with voltage driven nondestructive self-reference sensing scheme [13], the proposed comparator can provide a wider sense margin, as shown in Fig. 7.

IV. Conclusion

To conclude, we propose the IRRO cancellation technique for sense amplifiers. The spin-torque memristors can be connected in series or in parallel, but in series have less resistance and process variations than in parallel. In particular, the overwrite problem of the spin-torque memristor was solved by setting the critical switching current of the spin-torque memristor to be greater than a current value corresponding to maximum the IRRO value. We evaluated the IRRO cancellation technique on the proposed comparator or sense amplifier using 45nm predictive CMOS technology. Although sense amplifiers are targeted in this study, our technique can be applied to any analog amplifier suffering from the IRRO.

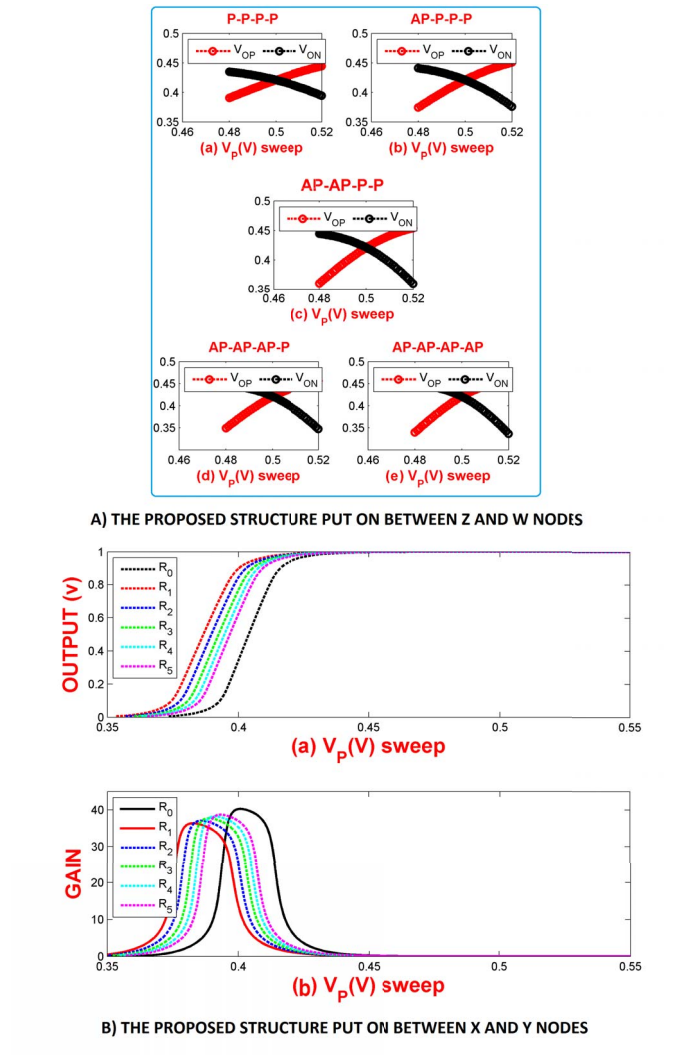

Fig. 6. The IRRO values and the gain of the voltage comparator adjustments with the spin-torque memristor.

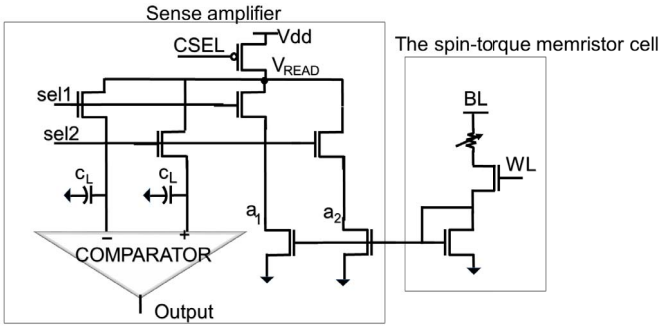

Fig. 7. The voltage driven nondestructive self-reference sense amplifier [13].

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