Behavioral Modeling for Low-Voltage Pentacene-Based OTFTs and Their Implementations for Organic Logic Circuits

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ABSTRACT

We present a behavioral compact model and its implementation for low-voltage pentacene-based organic thin film transistors (OTFTs) using industry standard BSIM4 (Berkeley Short-channel IGFET Model) in LTspice platform. First, we simplify the number of BSIM4 model parameters according to the device structure. On the other hand, we adapt the BSIM4 mobility equation to OTFT and also involve the off-current using two behavioral current sources. Then, we perform metaheuristics-based optimization to extract the related BSIM4 model parameters together with additional four parameters, introduced in this work, fitting the modified model to the experimental data of an OTFT, using pentacene active layer. Finally, we implement the behavioral compact model in LTspice and validate its usage for low-voltage pentacene-based OTFTs comparing the experimental and modeled current-voltage curves. In this study, we also successfully simulate OTFT implementations of a Pseudo-E inverter, a Pseudo-E NAND gate, and a 1-bit full adder circuit based on NAND gates using our behavioral OTFT model and then investigate the static and dynamic performance parameters of these circuits. The supply voltage is 3 V and maximum frequency of the inputs is 500 Hz in the simulations.

1. INTRODUCTION

Organic thin film transistor (OTFT) is an emerging technology which has promising application fields in flexible, large-area, and low-cost electronics such as ring oscillators and shift registers [1], digital logic gates, flip-flops, and full adder [2], [3], [4], digital-to-analog [5] and analog-to-digital [6] converters, an amplifier system [7], and an organic microprocessor [8].

As the application areas of OTFT-based circuits are increasing continuously, simulators such as SPICE with accurate compact models of OTFTs are becoming more important to design such circuits getting more complicated every passing day. There are even already articles in the literature presenting their organic electronic circuits involving thousands of transistors [8, 9]. In order to predict the electrical characteristics of these devices, OTFT-specific accurate compact models are necessary; however, there is not a standard model in SPICE simulators due to the lack of knowledge in device physics and diversity in the selection of device structures and organic materials which are evolving rapidly. Instead, researchers [10–14] adapt the other inorganic TFT or MOSFET models to make them suitable for the simulations of their organic electronic circuit designs. For instance, Meixner *et al.* [10] presented a Pspice model for OTFTs based on the standard BSIM (Berkeley Short-channel IGFET Model) equations. They modified the model equations by additional voltage-controlled current sources to involve the gate voltage dependence of the charge carrier mobility and the bulk conductivity according to their poly(3-hexylthiophene-2,5-diyl) (P3HT)-based OTFTs. In a preliminary work [15], we presented the Level 3 based model for low voltage pentacene based OTFTs. We thought that the Level 3 model could be more suitable for these large devices and it also has rather less parameters comparing to BSIM. However it has some disadvantages such as poor output conductance, weak subthreshold model and not capable of being scaled. We experienced these drawbacks in the simulations and decided to study with BSIM4 in this work. While the other researchers use commercially available SPICE simulators such as HSPICE, AIM-SPICE, and PSPICE, this article additionally presents a behavioral compact model in LTspice [16], a freeware SPICE simulator. It involves a subcircuit which adapts the simplified BSIM4 model to a pentacene-based OTFT manipulating its mobility equation according to the OTFT with a behavioral current source and inserting another one to include the off-current. Then, this subcircuit is used to simulate current-voltage (I-V) characteristics of the transistor and the usability of the model is validated showing that simulation results agree with the experimental data, taken from [17]. In this study, we contribute to the compact modeling efforts for OTFTs presenting a method to implement a recently proposed semi-empirical OTFT mobility formulation [18], covering both the subthreshold and above-threshold regimes. Thus, the drain current of the BSIM4 model can be adjusted according to the experimental data of the low-voltage pentacene-based OTFTs. The presented behavioral compact model is later used for digital electronic circuit simulations. Pseudo-E inverter and NAND gate configurations are implemented and simulated. After that a 1-bit full adder circuit using only NAND gates is implemented and simulated. The static and dynamic performance parameters are also investigated. In this work, we aim to benefit from BSIM4's robustness and its computationally efficient mathematical functions. The very large number of BSIM4 parameters are simplified according to the device structure; hence this process leads us to easier optimization of the most significant model parameters. This kind of simplified model can be the main body of a specialized parameter extractor to be used in OTFT researches and the nullified effects can be turned on through a user interface for the next fabrications, *e.g.* OTFTs with smaller channel lengths and widths. Therefore, this is another motivation of this work. As a result, this behavioral compact model based on BSIM4 is validated for the low-voltage pentacene-based OTFT data and some organic digital electronic circuits such as an inverter, a NAND gate, and

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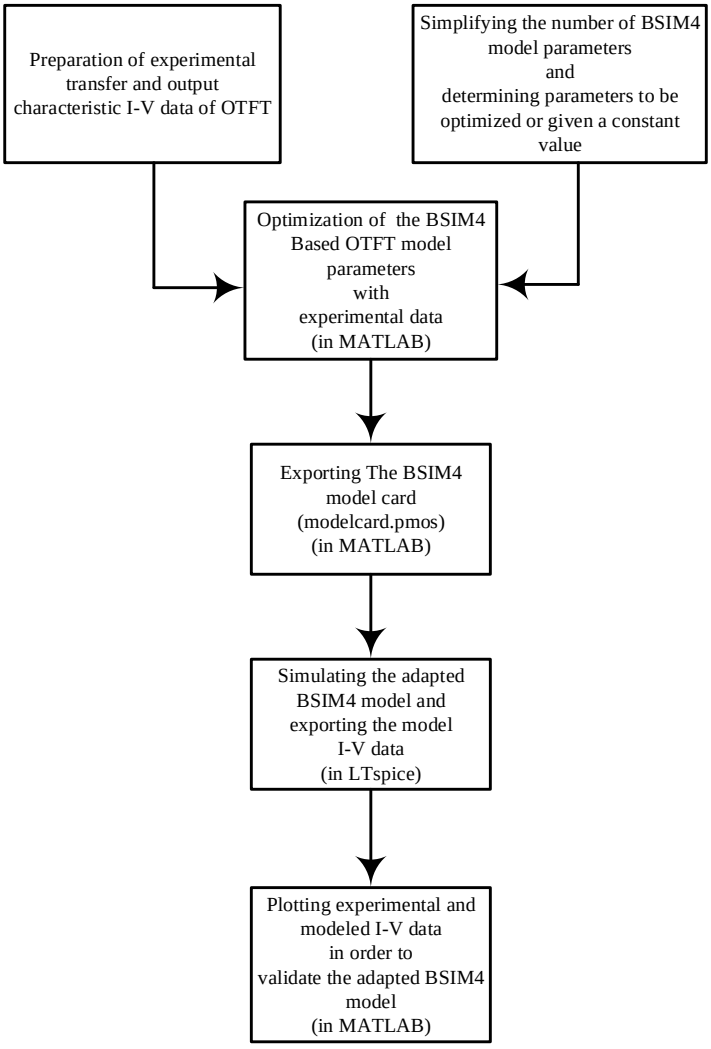


Fig. 1. The process flow of the adaptation of BSIM4 model for an OTFT from data collection step to model validation step

a 1-bit full adder are successfully implemented and simulated in LTspice environment with the help of this model. The organization of the rest of our article is as followed. Section 2 describes the presented behavioral model and the process of simplifying the number of model parameters. Section 3 gives the experimental results with discussions and finally, Section 4 concludes the article.

2. THE BEHAVIORAL OTFT MODEL

2.1. Simplifying the number of BSIM4 model parameters

A compact model is necessary to use OTFTs for circuit designs in SPICE tools. Since LTspice uses BSIM4.6.1 [19], known as Level 14, we use this version in this work. BSIM4 is a robust compact model and extensively used in the simulations of analog and digital designs. We simplify the number of BSIM4 model parameters in order to use this model effectively for low-voltage pentacene-based OTFTs. The flow from data collection to model validation is illustrated in Fig. 1.

In [20], the drain current expression of BSIM4 for all regions of operation is given in (1), where NF is the number of device fingers, $R_{ds}(V)$ is lightly doped drain (LDD) resistance, V_{ds} is the drain to source voltage, V_{dseff} is the effective drain to source voltage, C_{CLM} is the channel length modulation (CLM) coefficient, V_{Asat} is the Early voltage of device when $V_{ds} = V_{dsat}$ where V_{dsat} is the saturation voltage, V_A is written as $V_A = V_{Asat} + V_{ACLM}$ where V_{ACLM} is the Early voltage due to CLM, V_{ADIBL} is the Early voltage due to drain-induced barrier lowering (DIBL), V_{ADITS} is the Early voltage due to drain-induced threshold shift (DITS), and V_{ASCBE} is the Early voltage due to substrate current-induced body effect (SCBE). These effects and their detailed equations can be found in [19] and [20]. I_{ds0} is given by (2). Here W_{eff} and L_{eff} are respectively effective channel width and length; μ_{eff} is the effective field effect mobility; A_{bulk} is the bulk charge effect coefficient; v_t is the thermal voltage; V_{gsteff} is the effective and smoothing gate voltage where V_{gse} is the effective gate bias voltage containing the poly-Si gate depletion effect and V_{th} is the threshold voltage; finally E_{sat} is the critical electric field that allows the carrier velocity to be saturated. The poly-silicon gate depletion model is ignored in our case and V_{gse} is taken equal to V_{gs}.

The channel length modulation is taken into account in the second term of (1). This effect is insignificant due to device geometry and formation of the channel. In BSIM4, PCLM is the channel length modulation parameter and it is not allowed to be 0. The effects of different values of PCLM are insignificant according to simulations. Hence, it is removed from the model card and its default value will be used. Note that when a parameter is removed from the model card, its default value is still used by the functions in background. It is intented for just keeping the most significant parameters in the model card and making it simpler. The third term in (1) is related to DIBL effect. It is deduced from simulations that this effect is not negligible below threshold voltage for the OTFT used in this work. Subthreshold current is affected by DIBL. PDIBLCB, PVAG, PDIBLC1, PDIBLC2, and DROUT are model parameters to evaluate V_{ADIBL}. PDIBLCB is the body-bias dependence parameter. Since OTFT has no terminal for the body-bias, this terminal is connected to source and parameters related to the body effect are nullified in the BSIM4 model. With this information PDIBLCB would be nullified in the model card, however its default value is already 0. We may remove PDIBLCB from the model card. The other parameters are optimized. PDIBLC2 becomes effective for long channel devices and its value is usually very small. The fourth term in (1) is related to DITS effect. Pocket implants are used in modern MOS transistors. This causes threshold voltage shifts for long channel devices due to drain bias. OTFT has no pocket implants; hence, this effect should be nullified. It is not observed a significant difference during simulations with the default values of PDITS, PDITSL, PDITSD, FPROUT parameters. Therefore they may be removed from the model card. The last term in (1) comes from the SCBE. When this effect occurs, impact ionization current flows and contribute to the drain current. It reduces the threshold voltage because of the increased body potential and results with a larger drain current. Since the OTFT has no body, we can nullify this effect. The default values of PSCBE1 and PSCBE2 parameters show no effect on the simulations, so they may be removed from the model card for the sake of simplicity.

Smooth transitions among the regions of operation are modeled with the effective and smoothing drain to source voltage V_{dseff} and gate to source voltage V_{gsteff}. The mathematical expression of V_{dseff} is given in (3). Here, DELTA model parameter assists a smooth transition between the linear and saturation regions. The other expression for V_{gsteff} is given by (4), where n is the subthreshold swing parameter, $m^* = 0.5 + arctan(MINV)/\pi$ where MINV is a model parameter and improves the model accuracy, C_{dep0} is the depletion layer capacitance per unit area under zero body biases, and V^*_{off} is the offset voltage. The subthreshold swing parameter n is formulated by (5). Here, C_{dep} is the de-

$$I_{ds} = \frac{I_{ds0}\ NF}{1+\frac{R_{ds}(V)\ I_{ds0}}{Vdseff}} \left[1+\frac{1}{C_{CLM}}\ ln\left(\frac{V_A}{V_{Asat}}\right)\right] \left(1+\frac{V_{ds}-V_{dseff}}{V_{ADIBL}}\right) \left(1+\frac{V_{ds}-V_{dseff}}{V_{ADITS}}\right) \left(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}\right) \tag{1}$$

$$I_{ds0} = \frac{W_{eff}C_{oxeff}V_{gsteff}}{L_{eff}\left(1+\frac{V_{ds}}{E_{sat}L_{eff}}\right)}\ \mu_{eff}\ V_{ds} \left[1-\frac{A_{bulk}}{2(V_{gsteff}+2v_t)}\ V_{ds}\right] \tag{2}$$

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left[(V_{dsat}-V_{ds}-DELTA)+\sqrt{(V_{dsat}-V_{ds}-DELTA)^2+4\ DELTA\ V_{dsat}}\right] \tag{3}$$

$$V_{gsteff} = \frac{n\ v_t\ ln\left(1+exp\left[\frac{m^*\ (V_{gse}-V_{th})}{n\ v_t}\right]\right)}{m^*+n\ \frac{C_{oxeff}}{C_{dep0}}\ exp\left[-\frac{(1-m^*)(V_{gse}-V_{th})-V^*_{off}}{n\ v_t}\right]} \tag{4}$$

$$n = 1+NFACTOR\ \frac{C_{dep}}{C_{oxe}}+\frac{C_{dsc-term}+CIT}{C_{oxe}} \tag{5}$$

$$R_{ds}(V) = \frac{RDSWMIN+RDSW\ \left[PRWB\ (\sqrt{\phi_s-V_{bseff}}-\sqrt{\phi_s})+\frac{1}{1+PRWG\ V_{gsteff}}\right]}{(W_{effCJ}\ 10^6)^{WR}} \tag{6}$$

$$R_d(V) = \frac{RDWMIN+RDW\ \left[-PRWB\ V_{bd}+\frac{1}{1+PRWG\ (V_{gd}-V_{fbsd})}\right]}{(W_{effCJ}\ 10^6)^{WR}\ NF} \tag{7}$$

$$R_s(V) = \frac{RSWMIN+RSW\ \left[-PRWB\ V_{bs}+\frac{1}{1+PRWG\ (V_{gs}-V_{fbsd})}\right]}{(W_{effCJ}\ 10^6)^{WR}\ NF} \tag{8}$$

$$\mu_{eff} = \frac{U0\ \left(1-UP\ exp\left(\frac{-L_{eff}}{LP}\right)\right)}{1+\left[UA\ \left(\frac{V_{gsteff}+2V_t}{TOXE}\right)+UB\ \left(\frac{V_{gsteff}+2V_t}{TOXE}\right)^2\right]\ \left(1+UC\ V_{bseff}\right)+UD\ \left(\frac{V_t\ TOXE}{V_{gsteff}+2V_t}\right)^2} \tag{9}$$

pletion capacitance, NFACTOR is the coefficient for depletion capacitance dependence, C_{oxe} is the electrical gate oxide unit-area capacitance, and CIT is the parameter for interface trap capacitance. The OTFT has undoped pentacene layer hence, depletion region is not formed prior to conduction as stated for a similar case given in [21]. Therefore NFACTOR is set to 0. $C_{dsc-term}$ is introduced for the source/drain to channel coupling capacitance depending on channel length and its coefficients depending on body and drain bias voltages and it is related to model parameters of CDSC, CDSCB, CDSCD, and DVT1 [19]. This term is nullified when CDSC, CDSCB, and CDSCD parameters are set to 0. In this case, DVT1 becomes insignificant and it can be simply removed from the model card with CDSCB and CDSCD, having 0 default values. Consequently, n becomes dependent on solely CIT model parameter and it is optimized in this work.

In BSIM4, MTRLMOD is used to model for different types of gate and substrate materials. It is initially 0 for Poly Si/oxide/Si MOSFETs. In this work, MTRLMOD is set to 1 and this option is presented for new materials such as high-k metal gates and non-Si substrates. When metal gates are used, the relative dielectric constant of the gate, EPSRGATE, is set as 0 and there will be no gate depletion. The another parameter representing the doping concentration of poly-silicon gate, NGATE, will also be 0. Gate-channel tunneling currents are turned off by setting IGCMOD and IGBMOD flags to 0. RGATEMOD is the model selector for gate-resistance and set to 0 so that gate-resistance will not be generated. RBODYMOD is to generate body-resistance network. Its default value is 0 and this option is used in the simulations to exclude body-resistance model. GEOMOD and PERMOD are layout-dependence model selectors. They are set to 0. DIOMOD is source/drain-body junction diode current-voltage model selector. In OTFT simulations, DIOMOD is set to 0 and it has no effect on the drain current because $V_{bs} = 0$.

The resistance $R_{ds}(V)$ is taken into account when the BSIM4 model selector RDSMOD is equal to 0. On the other hand, it is split into $R_d(V)$ and $R_s(V)$ when RDSMOD is equal to 1. These resistance equations are given by (6), (7), and (8). In these equations, V_{bs} and V_{bd} are the body to source/drain voltages, V_{gs} and V_{gd} are the gate to source/drain voltages, V_{bseff} is the effective bulk to source voltage, RDSWMIN, RDWMIN, RSWMIN, RDSW, RDW, RSW, PRWB, PRWG, and WR are the model parameters. W_{effCJ} is the effective width of the drain and source diffusion and

```
.model   p1   pmos    level = 14
+version = 4.6.1   mobmod  = 1      mtrlmod  = 1      capmod  = 0
+igcmod  = 0       igbmod  =0       geomod   = 0      permod  = 0
+diomod  = 0       rdsmod  = 0      rgeomod  = 0
+rbodymod = 0      rgatemod = 0
+eot  = 4.94e-9    epsrgate = 0     a0 = 0            a1 = 0
+a2 = 0.011        cdsc = 0         cit = 0.0047
+vth0 = -1.22      k1  = 0          k2 = 0            k3 = 0
+kt1 = 0           kt1l = 0         dvt0 = 0          dvt1 = 0
+dvt2 = 0          dvt1w = 0        dvt2w = 0
+nfactor  = 0      minv = -0.6685   voff  = -0.2227
+ngate   = 0       ndep = 1.191e+19                   phin =  0
+u0 = 6.098e-05    etab     = 0     eta0  =  0
+ua  = 0           ub  = 0          uc    = 0         ud    = 0
+vsat  = 1550      pdiblc1 = 0.39   pdiblc2 = 0.0086
+pvag = 6990       delta = 0.1      drout  = 0.1079
+rdsw  = 3.137e+06                  rsw = 3.28e+06    rdw = 1.84e+06
+prwg = 0.7126                      wr  = 0.62
+cgso    = 7e-8    cgdo = 7e-8      cgbo    = 0
```

Fig. 2. BSIM4 (Level = 14) model card

ϕ_s is the surface potential. V_{fbsd} is the calculated flat-band voltage between gate and source/drain diffusion areas. PRWB is body-bias dependence coefficient. This parameter would be nullified due to non-existence of body terminal, but the default value is already 0. It may be removed from the model card for the sake of simplicity. PRWG is gate-bias dependence coefficient and its value is optimized in this work. If the source/drain contacts are assumed ohmic, then PRWG can be set to 0. WR is also optimized. RDSWMIN, RDWMIN, and RSWMIN are considered as their default values of 0 for simplicity and removed from the model card. The internal $R_{ds}(V)$ option is easier for using in our optimization algorithm. On the other hand, it is split into external resistances of $R_d(V)$ and $R_s(V)$ when the other option is chosen. We used both options but observed that RDSMOD=1 can be more useful in some transient simulations because it provides two resistances between the external and internal source and drain nodes. These resistances can also be modeled asymmetrically.

An another important model selector is CAPMOD. We set CAPMOD as 0 in our case because it is used for the transistors with long channels and it is also a simpler capacitance model. Here the new parameters such as CGSO, CGDO, and CGBO are introduced. These parameters are respectively the overlap capacitance for the gate-to-source, the gate-to-drain, and the gate-to-body and they are given in the unit of Farad per meter. Since there is no body terminal, CGBO is set to 0. The other parameters are calculated as follows:
$CGSO = CGDO = C_{oxe}L_{ov} = (7\times10^{-3})(10\times10^{-6}) = 7\times10^{-8}$ F/m. L_{ov} is used for the gate-to-source and the gate-to-drain overlap lengths assumed equal and this value was reported as $10\mu m$ in [17]. When CAPMOD=0 is chosen and CGSO, CGDO, and CGBO parameters are set as shown in our model card. The other parameters related to CAPMOD=1&2 such as CGSL, CGDL, CKAPPAS, and CKAPPAD are insignificant in simulations and they are removed from the BSIM4 model card. LTspice uses the default values of the other model selectors not included in the model card given in Fig. 2.

BSIM4 has a comprehensive threshold voltage model; however, the transistor studied in this work is a large device and threshold voltage is approximated to VTH0. The parameters related to threshold voltage shift due to short channel effects, non-uniform substrate doping, narrow width effects, and temperature dependence are nullified. Consequently, the following parameters are set to 0: K3, K3B, KT1, KT1L, KT2, DVT0, DVT0W, DVT2, DVT2W, DVTP0, DVTP1, ETA0, ETAB. The parameters which have 0 as default are K3B, DVT0W, DVTP0, DVTP1, and KT1L; hence these parameters can be removed from the model card. On the other hand, BSIM4 can model the effective channel length and width for the advanced CMOS process implementations. Unintentional process variations are modeled for the BSIM4 DC models and capacitance models with different sets of parameters such as XL, XW, LINT, WINT, DLC, DWC, DWG, DWB, and so on. We ignored these parameters for simplicity. Default values of these parameters are 0 and they can be removed from the model card. Instead, the effective channel width and length are taken equal to physical ones in this work. The parameters to be optimized are given in Table 1 and the constant parameters are given in Table 2. The other unmentioned model parameters, such as gate-induced drain/source leakage model parameters, impact ionization current model parameters, gate dielectric tunneling current model parameters, RF model parameters, flicker and thermal noise model parameters, etc., are insignificant and ignored in this work and removed from the model card. All of the parameters and related model equations can be found in [19] and [20].

Table 1
BSIM4 model parameters used for optimization.

Parameters	Definition
VTH0	Long channel threshold voltage at $V_{bs}=0$
NDEP	Channel doping concentrations
MINV	V_{gsteff} fitting parameter
VOFF	Offset voltage of the effective gate drive
PHIN	Offset parameter of surface potential due to non-uniform vertical doping
CIT	Interface trap capacitance
VSAT	Saturation velocity
U0	Low field mobility
PVAG	Gate-bias dependence of Early voltage
LAMBDA	Velocity overshoot coefficient
DELTA	Parameter for DC V_{dseff}
PDIBLC1	Parameter for DIBL effect on Rout
PDIBLC2	Another parameter for DIBL effect on Rout
DROUT	Channel length dependence of DIBL effect on Rout
PRWG	Gate bias dependence parameter of the lightly doped drain (LDD) resistances
RDSW	Zero bias source and drain LDD resistance component per unit width for RDSMOD=0
RDW	Zero bias lightly-doped drain resistance component per unit width for RDSMOD=1
RSW	Zero bias lightly-doped source resistance component per unit width for RDSMOD=1
WR	The power of the width dependence of source and drain LDD resistances

2.2. Adapting BSIM4 mobility model for OTFTs

Mobility model is extremely important to accurately model the device. The mobility model of MOBMOD = 1 is chosen as an example in this work and given by (9). As seen from the mobility equation, the effective mobility is inversely proportional to the gate voltage. However there are different counter examples for OTFTs. In [22], mobility equation for OTFTs is given by

$$\mu = \mu_0\left(\frac{V_{gs}-V_{th}}{V_{AA}}\right)^{\gamma} \tag{10}$$

where μ_0 is the zero-field mobility, V_{gs} is the gate to source voltage, γ and V_{AA} are fitting parameters to adjust mobility.

In [10], mobility is analytically approximated by

$$\mu = \mu_0 - \mu_1\, exp\,(V_{gs}/V_{\mu 0}) \tag{11}$$

where μ_1 and $V_{\mu 0}$ are model parameters.

A semi-empirical mobility model proposed in [18] is the last example given here and it is rewritten for p-type OTFTs as follows:

$$\mu = \frac{\mu_{sub}}{1+exp(-m_0V_{gt})} + \frac{\mu_{ab}}{1+exp(m_0V_{gt})}, \tag{12}$$

where μ_{ab} and μ_{sub} represent the mobilities in above- and sub-

Table 2
BSIM4 model parameters which are taken constant.

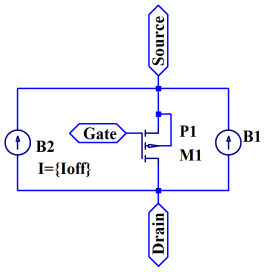
Parameters	Definition
NGATE	The doping concentration in the poly-silicon gate
VOFFL	Channel-length dependence of VOFF
EOT	Equivalent thickness of the gate oxide material for the MTRLMOD = 1
RDSWMIN	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0
RDWMIN	Lightly-doped drain resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
RSWMIN	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
NFACTOR	Subthreshold swing factor
PRWB	Body bias dependence parameter of the LDD source and drain resistances
CDSC	Coupling capacitance between source/drain and channel
K1	First-order body bias factor of the V_{th} model
K2	Second-order body bias factor of the V_{th} model for non-uniform vertical doping
UA	Gate bias dependence parameter for the effective mobility model
UB	Another gate bias dependence parameter for the effective mobility model
UC	Body bias dependence parameter for the effective mobility model
UD	Coulomb scattering dependence parameter for the effective mobility model
UP	Coefficient of the channel-length dependence of the low-field mobility U0

threshold regimes, respectively, and m_0 is a positive fitting parameter to connect them; $V_{gt} = V_{gs} - V_t$.

Using (10) causes problems with simulations. Abrupt transitions can be observed between below- and above-threshold regimes. On the other hand, (11) can be adapted to BSIM4 easily and it works in simulations without problems. In [10], the researchers worked with higher operating voltages from 0 up to –80V and validated (11) for P3HT-based transistors. In our work [15], (12) was tested and efficiently validated with the Level 3 MOSFET model for low voltage pentacene-based OTFTs. In fact, there is yet no universal mobility model for all organic semiconductor types, so we decided to adapt the BSIM4 MOSFET model to the studied low-voltage pentacene-based OTFTs according to (12), the more recent mobility expression among them, based upon our experience in [15]. In order to adapt the mobility equation of BSIM4, the model parameters UA, UB, UC, UD, and UP are first set to zero. In this case, LP parameter will become insignificant and it can be removed from the model card. Thus, (9) gives us simply U0 model parameter. After that (12) is implemented with a technique that uses a behavioral current source as shown in Fig. 3 to adjust the drain current evaluated by the BSIM4 model. I_{ds} will be proportional to $\mu_0 \times (\frac{A1}{1+exp(-A0\ V_{gt})} + \frac{A2}{1+exp(A0\ V_{gt})})$, where A0, A1, and A2 denote m_0, μ_{sub}/μ_0, and μ_{ab}/μ_0, respectively.

3. EXPERIMENTAL RESULTS

Fig. 3 presents the behavioral model consisting of a PMOS transistor and two behavioral current sources and it is applied to be able to model low-voltage pentacene-based OTFT. PMOS transistor is used with BSIM4 model card to predict I-V characteristics of OTFT, the behavioral current source is used to adapt the BSIM4 mobility expression to a more suitable one for the OTFT, and the other current source is used to include off-current of the transistor. BSIM4 has quite a lot parameters related to short channel and narrow width effects, leakage currents, different types of oxide and contact materials, and so on. We simplify these model parameters according to the studied OTFT structure and keep the most significant parameters for this case. In [17], the researchers fabricated this aforementioned OTFT in bottom-gate top-contact, *i.e.*



For B1:

I=Id(M1)*((A1/(1+exp(-A0*(V(Gate, Source)-Vt))))+(A2/(1+exp(A0*(V(Gate, Source)-Vt))))-1)

.include modelcard.pmos

.param Leff=10u Weff=100u Ioff=-5e-13 Vt = -1.22 A0=1.262 A1=0.4283 A2=1.138

Fig. 3. The schematic of the OTFT involving a PMOS transistor and two behavioral current sources in LTspice. Notice that BSIM4 model card is included and default values of the other parameters are defined in the subcircuit.

```
.subckt otft_pentacene Drain Gate Source
M1 Drain Gate Source Source P1 l={Leff} w={Weff}
B1 Drain Source I=Id(M1)*
+((A1/(1+exp(-A0*(V(Gate, Source)-Vt))))+(A2/(1+exp(A0*(V(Gate, Source)-Vt))))-1)
B2 Drain Source I={Ioff}
.include modelcard.pmos
.param Leff=10u Weff=100u Ioff=-5e-13 Vt = -1.22  A0=1.262  A1=0.4283  A2=1.138
.ends otft_pentacene
```

Fig. 4. The netlist for the subcircuit of the OTFT. Notice that BSIM4 model card is included and default values of the other parameters are defined in the subcircuit.

inverted staggered, device structure with patterned metal gate. Vacuum-deposited pentacene is used as a semiconducting active layer and a thin film of aluminum oxide is used as a gate dielectric material which provides a gate oxide capacitance per area of 0.7 $\mu F/cm^2$. They reported that the device has a channel length and width of 10 μm and 100 μm, respectively, a carrier mobility of 0.4 cm^2/Vs, and a threshold voltage of $-1.2\ V$.

3.1. Model validation

We have four output characteristic curves of OTFT, taken by sweeping V_{ds} from 0 to $-3\ V$ with steps of $-0.05\ V$ when V_{gs} was set to $-1.5\ V$, $-2.1\ V$, $-2.7\ V$, and $-3\ V$, and two transfer curves of OTFT, taken by sweeping V_{gs} from 0 to $-3\ V$ with steps of $-0.05\ V$ when V_{ds} was set to $-0.1\ V$ and $-1.5\ V$. In order to predict these transistor characteristic curves using the proposed model given in Fig. 3, we first set constant parameters and then run the metaheuristics-based optimizer, which we present in [23], in MATLAB and extract the parameters which appear in the BSIM4 model card. Here, (1) is the main cost function and the BSIM4 model parameters are optimized using all the experimental data. We note that LTspice adds a current value of $Gmin \times V_{ds}$ to the drain current of the transistor. Initial value of $Gmin$ is defined as 1E-12 in LTspice control panel and this parameter causes problems with fitting drain current in the subthreshold region and decreases accuracy if it is not taken into account. We set $Gmin$ as 1E-13 in our simulations. On the other hand, the off-current value is fixed to 5E-13 using a behavioral current source given in Fig. 3. When $V_{gs} = 0$, the off-state drain current is reported as about 0.5 pA in [17]. Therefore, we set a constant value of 5E-13 for the parameter I_{off}. A MATLAB script is written that exports the model card including all parameters to a text file as given in Fig. 2 and then this model card can be used for PMOS transistor on schematic shown in Fig. 3 or in netlist of the subcircuit given in Fig. 4. All the model parameters used in optimization process are given in Table 1. As given in [17], the oxide thickness is 5.7 nm and the gate oxide capacitance per area is 0.7 $\mu F/cm^2$. Using these values,

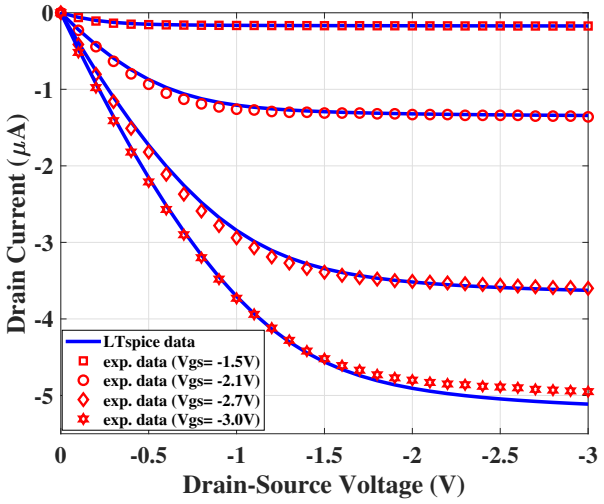


Fig. 5. Comparison of experimental and modeled output characteristics of the OTFT for V_{gs} = –1.5 V, –2.1 V, –2.7 V, and –3 V. The physical channel length and width are 10 μm and 100 μm, respectively.

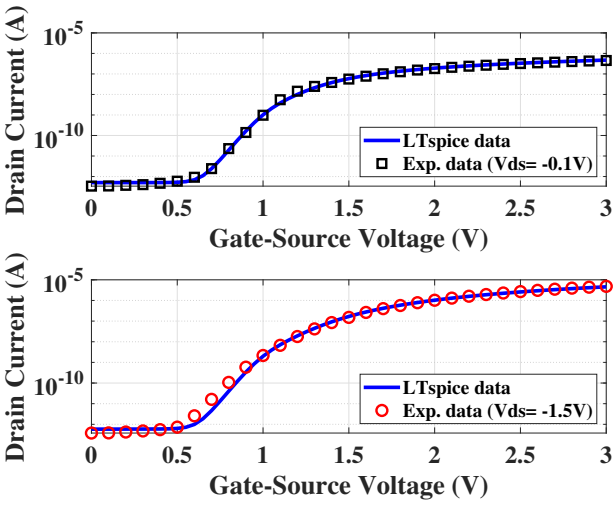


Fig. 6. Comparison of experimental and modeled transfer characteristics of the OTFT for V_{ds} = –0.1 V and –1.5 V. The physical channel length and width are 10 μm and 100 μm, respectively.

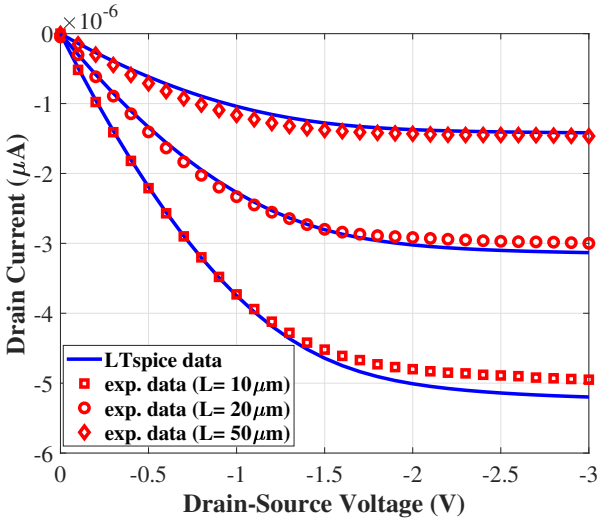


Fig. 7. Comparison of experimental and modeled output characteristics of the OTFTs having physical channel lengths of 10μm, 20μm, and 50μm when V_{gs} = –3 V.

the relative permittivity of the gate dielectric can be calculated as 4.5. When MTRLMOD flag is 1, EPSROX model parameter for the relative permittivity of the gate dielectric is assumed as silicon dioxide's relative permittivity of 3.9. In this case, the effective oxide thickness parameter of EOT is introduced and its value is calculated by scaling the oxide thickness of the OTFT with 3.9/4.5. EOT replaces TOXE. The effecive channel lengths are taken equal to the physical lengths of 10 μm, 20 μm, and 50 μm.

After optimization of model parameters, threshold voltage is found as $-1.22\ V$ and the maximum mobility is calculated from (12) as 6.53e-5 m^2/Vs when $V_{gs} = -3\ V$. In the following step, DC simulations of the adapted BSIM4 model are performed in LTspice platform according to the sweeping conditions of the experimental data. Then, the simulated data is exported to a text file and the experimental and simulation data are compared by plotting both of them using a MATLAB script. Fig. 5 gives the modeled output curves that accurately agree with the experimental data and Fig. 6 gives the comparison of transfer characteristic curves. The output conductance and the transconductance (g_m) values are respectively reported as 100 nS and 4 μS in [17]. In Fig. 5, the differential output conductance ($\partial Id/\partial V_{ds}$) can be calculated as 106.51 nS when $V_{gs} = -3\ V$ and $V_{ds} \to -3\ V$. In Fig. 6, the maximum transconductance ($g_m = \partial Id/\partial V_{gs}$) is calculated as 4.16 μS when $V_{ds} = -1.5\ V$ and $V_{gs} \to -3\ V$. Fig. 7 presents the ouput curves of the OTFTs havig the physical channel lengths of 10 μm, 20 μm, and 50 μm when V_{gs} is set to –3 V. This figure shows that the behavioral model can be scalable when appropriate parameters are extracted and set. As seen in these figures, the model shows a good performance for the transfer and output data of the low-voltage pentacene-based OTFTs and it is validated for the gate and drain voltages ranging from 0 to –3V.

3.2. Simulation performance

After validation process, we want to show simulation performance of the presented behavioral OTFT model for some digital electronic circuits. We implement an inverter, a 2-input NAND gate, and a 1-bit full adder circuit using Pseudo-E design with p-type pentacene-based OTFTs. In this work, Pseudo-E design is selected in the light of researches in the literature [3, 24–26] because it provides rail to rail output voltage swing and it has a more controllable and desirable performance although it requires twice the transistor count [24]. Fig. 8 presents the schematic of the Pseudo-E inverter circuit configuration together with the logic symbol and truth table of that. In this inverter configuration, the inverter circuit has two stages. M_1 and M_{UP} are the driver transistors and the gate electrodes of them are wired to the input voltage (V_{in}) while the output node of the first stage is wired to the gate electrode of M_{DP}, the load transistor of the second stage. When the input is low, the driver transistors pull the output to high simultaneously. Hence the output node voltage of the first stage (V_{IM}) is pulled to high so M_{DP} becomes off and prevents a direct current from V_{DD} to ground in the second stage. V_{SS} voltage can be used to control the pull-down force with M_2 adjusting V_{IM} and it can improve the circuit yield and reliability. In all simulations, the supply voltage (V_{DD}) is 3 V and the bias voltage (V_{SS}) is -3 V. An oscilloscope impedance (1 MΩ // 16 pF) is assumed as a load at the output node. The channel width of the driver transistor is designed larger than the load transistor to increase output swing. While the channel widths of the load and driver transistors are respectively 100 μm and 400 μm, the channel lengths are 10 μm for both transistors. The voltage transfer characteristic of the designed inverter is as shown in Fig. 9 and the transient behavior of it is as shown in Fig. 10. The output voltage swing (VS) is obtained as 2.99 V. The noise margin low (NML) and the noise

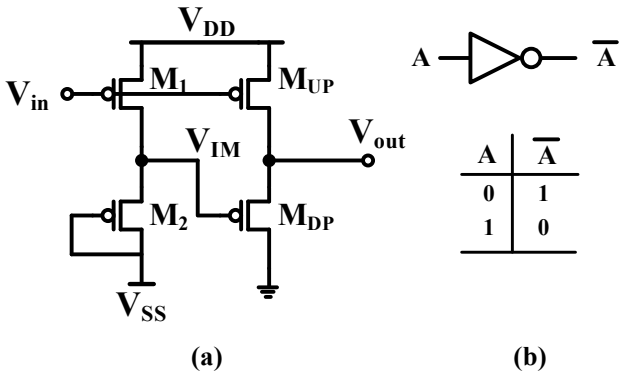


Fig. 8. (a)The schematic of the inverter circuit based on the Pseudo-E design. (b) Logic symbol and truth table of the inverter.

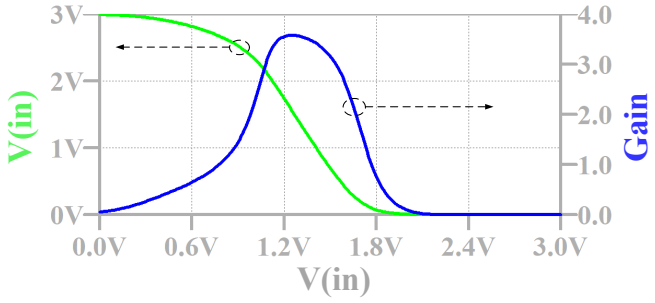


Fig. 9. The voltage transfer characteristic of the inverter circuit based on the Pseudo-E design. The channel lengths of all OTFTs are 10 μm. The channel widths of the load and driver transistors are 100 μm and 400 μm, respectively. V_{SS} = -3.0 V.

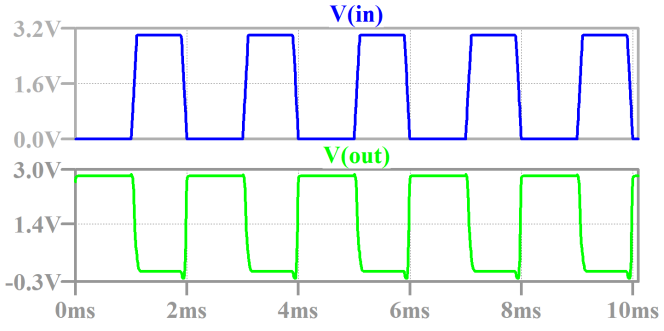


Fig. 10. The transient behavior of the inverter circuit based on the Pseudo-E design. The channel lengths of all OTFTs are 10 μm. The channel widths of the load and driver transistors are 100 μm and 400 μm, respectively. V_{SS} = -3.0 V. The load at the output node is 1 MΩ // 16 pF in the simulation.

margin high (NMH) values can be found by evaluating the -1 slope points on Fig. 9 using a graphical approach [27] and they are obtained as 0.68 V and 0.91 V, respectively. The mid-point voltage (V_M=V_{in}=V_{out}) is 1.32 V and gain ($-\partial V_{out}/\partial V_{in}$) is 3.55. The dynamic characteristics such as rise time (τ_{rise}), fall time (τ_{fall}), low-to-high propagation delay (τ_{PLH}), high-to-low propagation delay (τ_{PHL}), and average propagation delay (τ_P) is found as 29.22 μs, 75.84 μs, 32.66 μs, 10.87 μs, and 21.77 μs, respectively. The average power consumption is also calculated as 54.11 μW for this inverter configuration. These static and dynamic performance parameters are given in Table 3.

Fig. 11 presents the schematic of Pseudo-E 2-input NAND circuit configuration together with the logic symbol and truth table

Table 3
The static and dynamic performance parameters of the inverter.

VS (V)	NML (V)	NMH (V)	Gain	P_{avg} (μW)
2.99	0.68	0.91	3.55	54.11
τ_{rise} (μs)	τ_{fall} (μs)	τ_{PHL} (μs)	τ_{PLH} (μs)	τ_P (μs)
29.22	75.84	10.87	32.66	21.77

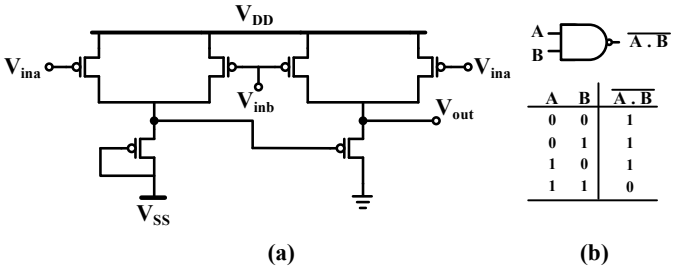


Fig. 11. (a)The schematic of the NAND circuit based on the Pseudo-E design. (b) Logic symbol and truth table of the NAND gate.

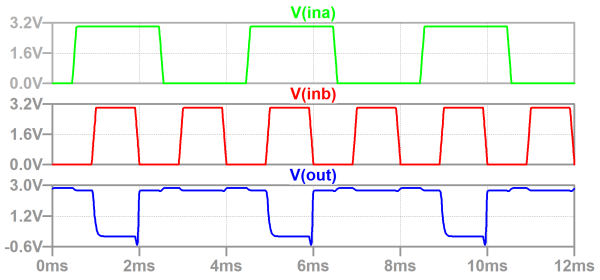


Fig. 12. The transient simulation of the NAND circuit based on the Pseudo-E design. The channel lengths of all OTFTs are 10 μm. The channel widths of the load and driver transistors are 100 μm and 400 μm, respectively. V_{SS} = -3.0 V. The load at the output node is 1 MΩ // 16 pF in the simulation.

of this logic gate. The channel widths and lengths of the transistors, the supply and bias voltages are the same as in the inverter case. Fig. 12 shows the transient simulation result of this 2-input NAND circuit. The frequencies of A and B inputs (V_{ina} and V_{inb}) are 250 Hz and 500 Hz, respectively. As seen in this figure the output voltage (V_{out}) matches the NAND gate Boolean function ($\overline{A \cdot B}$). When both inputs are logic "1" and the pull-up network is not conducting, the output is discharging through the load transistor and becomes logic "0". Otherwise, the pull-up network is conducting and thus the output node is charged and observed as logic "1". It can also be observed that when both inputs are low the output node is strongly pulled up and V_{out} has slightly higher voltage level. The average power consumption for this NAND gate is calculated as 87.53 μW and the worst-case propagation delay is found as 35.67 μs.

After designing the NAND gate, we implement a 1-bit full adder, a basic computing unit of a microprocessor, using 9 NAND gates having 54 OTFTs to see performance of multiple NAND gates connected in a circuit. Fig. 13 presents the full adder circuit designed with only NAND gates. This circuit has three 1-bit inputs of A, B, and the carry-in (C_{in}) and two 1-bit outputs of sum (S) and carry-out (C_{out}). Fig. 14 presents the transient simulation results of the circuit. The frequencies of the inputs of A, B, and C_{in} are respectively 500 Hz, 250 Hz, and 125 Hz. It can be observed in Fig. 14 that the waveforms match exactly with the full adder Boolean equations' results ("$S = A \oplus B \oplus C_{in}$", "$C_{out} = A \cdot B + C_{in} \cdot (A \oplus B)$"). For instance, when $A = B = "0"$ and $C_{in} = "1"$, it gives $S = "1"$ and $C_{out} = "0"$ or when $A = "1", B = "0"$ and $C_{in} = "1"$, it gives $S = "0"$ and $C_{out} = "1"$. In the shaded area, logic "0" and logic "1" values are indicated and truth table of the

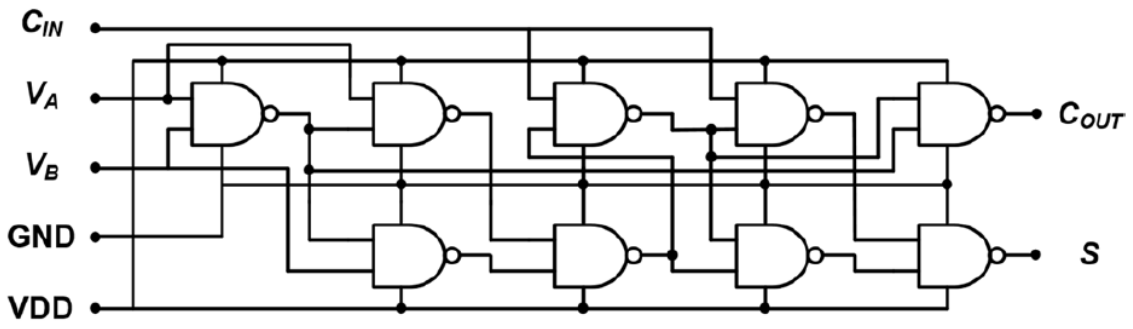


Fig. 13. The full adder circuit realization using nine NAND gates.

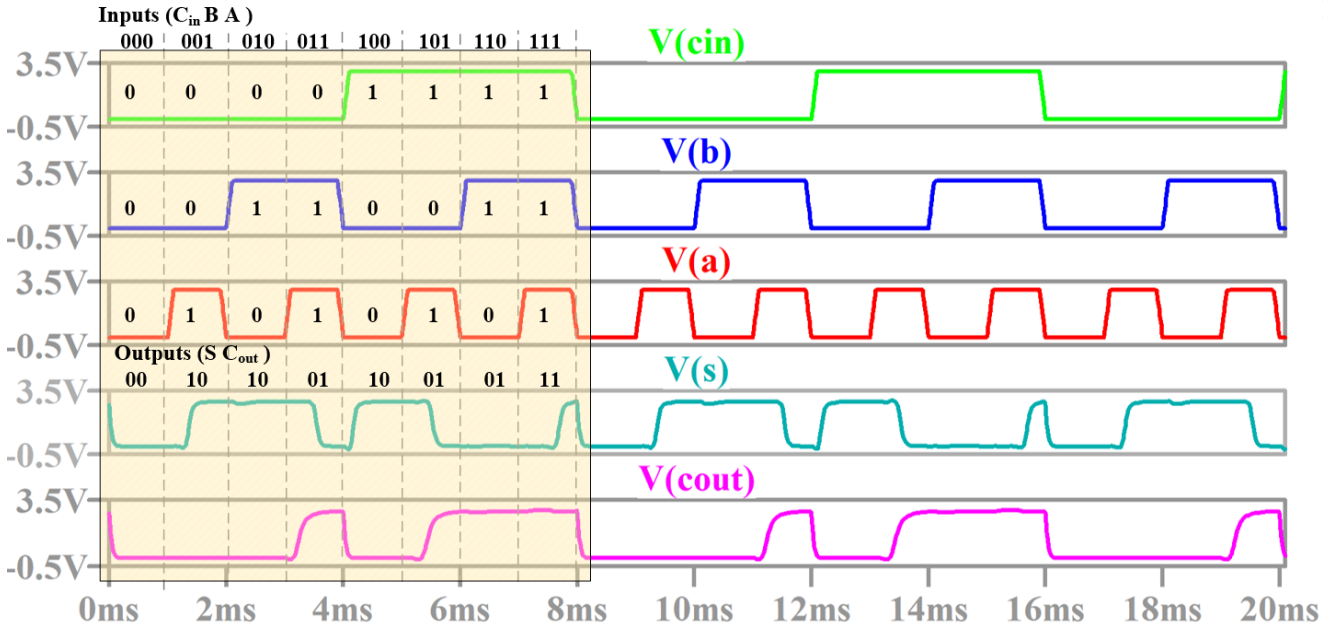


Fig. 14. The transient behavior of the 1- bit full adder circuit. The logic levels are indicated in the shaded area for the verification of the full adder's truth table. The channel lengths of all OTFTs are 10 μm. The channel widths of the load and driver transistors are 100 μm and 400 μm, respectively. V_{SS} = -3.0 V. The loads at the output nodes are 1 MΩ // 16 pF in the simulation.

full adder can be verified easily on the plot. The average power consumption of this full adder circuit is calculated as 533.04 μW. The worst-case propagation delays for the sum and carry-out outputs are found as 646.06 μs and 404.96 μs, respectively. Here once again we note that an oscilloscope impedance (1 MΩ // 16 pF) is assumed as a load for the output nodes in the transient simulations.

4. CONCLUSION

In conclusion, we present a behavioral BSIM4-based compact model to predict the characteristics of low-voltage pentacene-based OTFTs. We benefit from BSIM4's computationally efficient mathematical functions and convergence robustness. This model is implemented in LTspice as a subcircuit involving a PMOS transistor, two behavioral current sources and introducing additional four parameters alongside the existing ones for the simplified BSIM4 model. Although BSIM4 model parameters are simplified, the model data agree well with the experimental transfer and output characteristic data of the OTFT. After the model is validated for the gate and drain voltages ranging from 0 to –3V, we successfully perform DC and transient digital electronic circuit simulations in LTspice including a Pseudo-E inverter, a Pseudo-E NAND gate, and a 1-bit full adder using only NAND gates. The static and dynamic performance parameters are investigated. The circuits operate at a 3 V supply voltage and the maximum frequency for inputs is set to 500 Hz. As a result, the presented behavioral OTFT model is validated for pentacene-based OTFTs operating at low voltages and shows a satisfying performance for the simulations of the organic digital electronic circuits implemented by these transistors. In future works, this model can be extended to other kinds of device structures, organic semiconductors, and gate dielectrics, then it can be very helpful for the design and simulation phases of practical OTFT circuits in preliminary works. A specialized parameter extractor can also be built for the OTFTs based on this model.

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