Low Input Resistance Current Buffer Stage Using a Controllable Positive Feedback Loop, and Applications of Current Conveyor Based Filters

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Abstract

A novel current buffer stage with very low input resistance is proposed. Low input resistance is achieved using a potentially instable positive feedback loop. Stability of the circuit under different operating conditions is examined in details. A feedback control block using a bipolar 4-bit current steering DAC as a control mechanism is added to the buffer to control the input resistance and assure stability. The proposed technology-independent design methodology always ensures precision and stability for all different parasitic capacitor and resistor values of the driving signal source as well as for process, mismatch, and environmental variations. Additionally, a novel second generation current conveyor circuit based on this novel input buffer is presented to demonstrate how this buffer makes almost ideal current mode circuits possible. Filter applications using the proposed CCII are performed for further justification. The current buffer and CCII were built in AMS 0.35 μm 2P4M CMOS technology. Measurement results are presented for the current buffer, the CCII circuit, and the filters.

1. Introduction

Analog signal processing is traditionally done in voltage domain. To process analog current signals, current to voltage conversion is usually performed. Current detectors, readout circuits, and sensors first convert input current signals to voltage signals using relatively costly resistors and amplifiers, and then process voltage signals [1–3]. This overhead is much more severe if smaller current levels need to be sensed since larger resistors are needed. Moreover, larger resistors result in larger noise in circuit inputs. To eliminate this problem, one can directly use the current input without a conversion, so a current mode operation is needed.

Current mode operation is beneficial in predominantly capacitive IC environment due to maximized speed and minimized voltage swing [4–6]. A major factor limiting the speed of voltage mode signals is the time needed to charge and discharge parasitic capacitances at the internal nodes as the node voltages swing [5]. Since the voltage swings in current mode circuits are reduced, voltage changes across parasitic capacitances will be less. Moreover, lower node impedances will decrease time constants of internal nodes [7]. Therefore, internal nodes will settle faster in current mode circuits compared to voltage mode circuits. Reduced voltage swings at internal nodes will also decrease dynamic power consumption at high speed operation. Smaller voltage swings also decrease cross talk and switching noise. Current mode circuits can achieve higher dynamic range at lower supply voltages since the circuit performance is not limited by maximum voltage swing [8,9]. Simplicity of arithmetic operations is another advantage of current mode signal processing over voltage mode signal processing. Addition or subtraction can be achieved simply by connecting output nodes together and simple current mirrors can achieve scaling [9].

Although current mode circuits have significant advantages as mentioned, there are still problems to be solved, and the most important one is the difficulty of achieving low, ideally zero, input resistances. Consider a conventional current input stage such that source of a MOSFET or emitter of a BJT is used as an input node to achieve low input resistance. Here, the resistance value is roughly reciprocal of the transistor transconductance value ($1/g_m$) that is in the order of kilo ohms for MOSFETs. Unless the driving circuit has an output resistance much higher than $1/g_m$, the accuracy of this current input stage is not satisfactory. Moreover, transconductance is nonlinear. Since g_m depends on current and transistor size, achieving a small input resistance requires increasing current or transistor size. Increasing current will increase power consumption and increasing transistor size will increase parasitic capacitances and slow the circuit down.

A well-known solution to this problem is exploiting negative feedback [6,10]. Negative feedback loop decreases the input resistance by the feedback loop gain. However, negative feedback introduces problems such as extra parasitic capacitance and power consumption. Reducing the input resistance significantly requires a very large gain amplifier. The added amplifier dramatically worsens area, power, and speed performance of the whole circuit. Moreover, in order to avoid an addition of pole-zero doublet, the local feedback loop must have much higher gain bandwidth product than that of main loop [6].

An alternative approach for reducing input impedance is to use positive feedback [11–14]. Positive feedback decreases input resistance by applying series feedback to the input node. The current input stage with positive feedback was first proposed by Sedra in 1968 as the main building block of the first generation current conveyor (CCI) and was built with BJTs. Additionally, class AB amplifiers based on the CCI were proposed for buffering and amplifying bidirectional input currents [12,15]. However, these circuits suffer from poorly biased quiescent current. To fix the quiescent current problem, an AB amplifier using a translinear loop and 3 current carrying branches was proposed [16]. Nevertheless, none of these studies guarantees precision of the input resistance. Moreover, positive feedback can potentially cause instability and none of these studies analyzes stability of the input stage. We overcome these problems by proposing a very low resistance, precise, and stable current buffer stage with a controllable positive feedback loop. We also introduce a novel second generation current conveyor (CCII) circuit based on the proposed input buffer. Filter applications are given for further justification. Both the input buffer and the current conveyor were built in AMS 0.35 μm 2P4M process. Simulated performance was verified with measurement results.

The paper is organized as follows. Section 2 describes the proposed current buffer. Section 3 describes the proposed CCII. Section 4 presents filter applications using the current conveyor. Section 5 presents simulation and measurement results and Section 6 is the conclusion.

2. Proposed Current Buffer

The proposed current buffer is shown in *Figure 1*. It has 30 μA bias current with class A configuration. Therefore, input dynamic range is limited with this bias current if the input current is injected. However, when the current is drawn, the limiting factor is power supply and the reference voltage V_{REF} selected as $V_{DD}/2$. Thus, power supply must be at least $V_{REF}+V_{DSAT}+V_{GS}$. Maximum and minimum currents for proposed buffer is given in (1):

$$\sqrt{\frac{2I_{D1,2,3,4}}{K}} + V_{th} + \frac{V_{DD}}{2} + V_{DSAT} \le V_{DD} \qquad (1)$$
$$-493\,\mu A \le I_{D1,2,3,4} \le 30\,\mu A$$

where K is equal to $\frac{1}{2}\mu_n C_{ox} W/L$. For our design V_{DD} = 3V, V_{th}=0.7V, V_{DSAT}=150mV, and $\mu_n C_{ox} W/L = 2334\mu A/V^2$. Transistor dimensions for current buffer are given in Table 1.

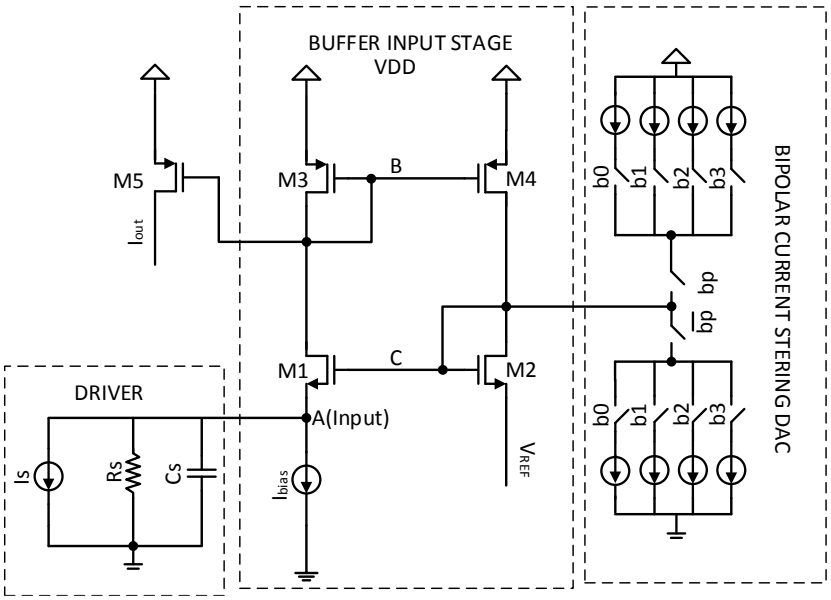


Figure 1. The proposed CMOS current buffer circuit

Table 1. Transistor Dimensions for Proposed Current Buffer

Transistor	W(μm)	L(μm)
M1	11	1
M2,5	10	1
M3,4	30	1

The current buffer has a very low input resistance and its feedback is controlled to keep the buffer stable. The input impedance looking toward the A node without considering the driver is given in (2):

$$Z_{in}(s)=\frac{s^2\left(C_{gs1}+C_c\right)C_b+s\left(\left(g_b+g_{ds1}\right)\left(C_{gs1}+C_c\right)+g_cC_b\right)+\left(\left(g_b+g_{ds1}\right)g_c-g_{m1}g_{m4}\right)}{s^3\left(C_{gs1}C_bC_c\right)+s^2\left[\left(g_c+g_{ds1}\right)C_bC_{gs1}+\left(g_b+g_{ds1}\right)C_cC_{gs1}+\left(g_{m1}+g_{ds1}\right)C_bC_c\right]} \\ +s\left[\left(g_{m1}+g_{ds1}\right)\left(g_bC_c+g_cC_b\right)+C_{gs1}\left(g_{ds1}\left(g_{m4}+g_b+g_c\right)+g_bg_c\right)\right]+\left(g_{m1}+g_{ds1}\right)g_bg_c \quad (2)$$

$$g_b=g_{m3}+g_{ds3} \qquad g_c=g_{m2}+g_{ds2}+g_{ds4}$$

$$C_b=C_{gs3}+C_{gs4}+C_{gs5}+C_{db1}+C_{db3} \qquad C_c=C_{gs1}+C_{gs2}+C_{gs3}+C_{db4}+C_{db2}$$

where C_b and C_c are the parasitic capacitances at nodes labelled B and C, and g_b and g_c are equivalent conductances at nodes B and C. The input resistance of the circuit is given in (3).

$$R_{in}=Z_{in}(0)=\frac{\left(\left(g_b+g_{ds1}\right)g_c-g_{m1}g_{m4}\right)}{\left(g_{m1}+g_{ds1}\right)g_bg_c}\cong\frac{1}{g_{m1}+g_{ds1}}\left(1-\frac{g_{m1}g_{m4}}{\left(g_b+g_{ds1}\right)g_c}\right)=\frac{1}{g_{m1}+g_{ds1}}\left[1-L(0)\right] \quad (3)$$

Equation 3 shows that series-shunt positive feedback decreases the input resistance by a factor of (1- $L(0)$) where $L(0)$ is the DC gain of the internal feedback loop formed by M1-M4 excluding any impedance connected to the input. Since $g_bg_c > g_{m1}g_{m4}$ when the NMOS and PMOS transistors are perfectly matched, L(0) will be smaller than 1, so the input resistance will be positive. However, mismatch between transistors can result in a loop gain larger than unity. For instance if aspect ratio of M1 turns out to be larger than M2 or M4 turns out to be larger than M3, L(0) might be larger than unity. This will lead to instability. Therefore, using this circuit requires a careful stability analysis because of positive feedback.

Proposed circuit has three parts: driver, buffer, and digital to analog converter as shown in *Figure 1*. Source of M2 transistor is connected to a reference voltage. Source of M1 transistor is the input node. A current source connected to the input node biases the buffer.

The feedback loop gain is given in (4):

$$L' = \frac{g_{m1}g_{m4}}{g_b g_c}\left(\frac{R_o \| R_s \| (1/g_{m1})}{R_o \| R_s}\right)\frac{1 + sC_s(R_o \| R_s)}{(1 + s(C_b/g_b))(1 + s(C_c/g_c))(1 + sC_s(R_o \| R_s \| (1/g_{m1})))} \tag{4}$$

$$L' = \frac{g_{m1}g_{m4}}{(g_b + sC_b)(g_c + sC_c)}\frac{1}{g_{m1}Z_x + 1} = L\frac{1}{g_{m1}Z_x + 1} \qquad L = \frac{g_{m1}g_{m4}}{g_b g_c}\frac{1}{(1 + s(C_b/g_b))(1 + s(C_c/g_c))}$$

where R_o is the output resistance of the bias current source, R_s and C_s are the output resistance and capacitance of the signal source that drives the circuit; L' is the loop gain of the circuit considering R_o, R_s and C_s. It is evident from Equation 4 that the signal source introduces an additional pole and a zero to the overall loop gain $L'(s)$. The pole and zero added by the signal the source are given in (5).

$$\omega_{zA} = \frac{1}{C_s(R_o \| R_s)} \qquad \omega_{pA} = \frac{1}{C_s(R_o \| R_s \| (1/g_{m1}))} \tag{5}$$

The zero frequency is lower than the pole frequency. Therefore, the zero-pole pair increases the magnitude of loop gain depending on the separation of the zero and the pole. Since $R_o >> 1/g_{m1}$, seperation of zero and the pole depends on the relative sizes of R_s and $1/g_{m1}$. For Cs values larger than transistor parasitic capacitances, the two poles of loop gain $L(s)$ are at higher frequencies, and the zero and the pole introduced by signal source dominate the frequency response at lower frequencies. In frequency domain, zero ω_{zA} comes first, leading to an increase in magnitude and phase. Assuming C_s is much larger than C_B and C_C, ω_{pA} comes after ω_{zA} and cancels the effects of ω_{zA} on magnitude and phase at approximately ω_{pA}. If there were no other poles, and magnitude of L' would stay constant. If L' reaches 1 between zero and pole, it would stay larger than 1. Fortunately, open loop gain of the buffer excluding R_o and Z_s has 2 poles. These two poles are given in (6).

$$\omega_{pB} = \frac{g_b}{C_b} \qquad \omega_{pC} = \frac{g_c}{C_c} \tag{6}$$

Equation 6 shows that $L'(0) < L(0)$, but overall loop gain can be larger than 1 for some frequencies because of the zero. The circuit would absolutely oscillate if magnitude of $L'>1$ and total phase shift of L' is equal to 0 at frequencies above ω_{pA}. Fortunately, parasitic capacitances at node B and C can prevent unstability if their pole frequencies are close enough to ω_{pA}, preventing L' from reaching 1. Signal sources, which have relatively large capacitances or very small resistances, can potentially cause instability. Thus for a comprehensive stability analysis, we need to consider effects of C_s and R_s.

When $L(0) <1$, the circuit is stable for all signal source impedances. However, $L(0)$ must be as close to 1 as possible to achieve very small input resistance. Even if the input buffer is designed for a loop gain close to, but less than 1, loop gain $L(0)$ might end up larger than 1 after manufacturing due to transistor mismatches. Therefore, stability of the circuit when $L(0)$ is slightly larger than 1 must be studied. For $L(0) > 1$, we need to check different cases for stability.

The first case considers very small values of R_s such that $R_s<<1/g_{m1}$. In this case R_s removes negative feedback effect of R_o, so $L'(0)\approx L(0)$. Since $L >1$ and $L' >1$, the circuit always oscillates. The second case considers values of R_s much larger than $1/g_{m1}$. R_o is also much larger than $1/g_{m1}$. In this case, $L'(0)$ is much lower than unity. However, the zero moves to a lower frequency as well and $L'(s)$ will approach $L(s)$ as frequency approaches pole frequency ω_{pA}. If C_s is comparable to the transistor parasitic capacitances at nodes B and C, the other two poles ω_{pB} and ω_{pC} will be close to the pole frequency ω_{pA}, and $L(s)$ will decrease below $L(0)$ at ω_{pA}. Therefore, overall loop gain $L'(s)$ can be less than 1 even at ω_{pA} frequency. However, if C_s has a large value, ω_{pA} will be much smaller than the other two poles. In this case $L(j\omega_{pA})\approx L(0)>1$. Therefore, L' will be greater than 1 leading to unstability. So, it is useful to determine the maximum value that C_s can get. Maximum value of C_s depends on the parasitic capacitances at nodes B and C and $L(0)$. In our test setup, C_b was set to $3C_c$ and $L(0)$ was set to 1.05; frequency sweeps for different values of C_s were performed and maximum value of $L'(s)$ was obtained for

each C_s value. *Figure 2* shows the results for different values of $k=C_s/C_b$. If k is less than 65, $L'(s)$ is less than 1 for all frequencies in this setup. This means when $R_s >> 1/g_{m1}$, the circuit can be stable if $C_s < 65\ C_b$ in this setup.

The last case is when the driving sources has resistance comparable to $1/g_{m1}$. In this case, ω_{pA} depends on both g_{m1} and R_s. Since ω_{zA} and ω_{pA} vary with R_s, obtaining an explicit mathematical expression is not easy. Once again C_b was set to $3C_c$, $L(0)$ was set to 1.05, and $1/g_{m1}$ is set to approximately 3k. The maximum value of C_s that assures $L'(s)$ to be less than 1 for all frequencies is determined for different values of signal source resistance. *Figure 3* shows the maximum value of the capacitor ratio k for different values of R_s to assure stability.

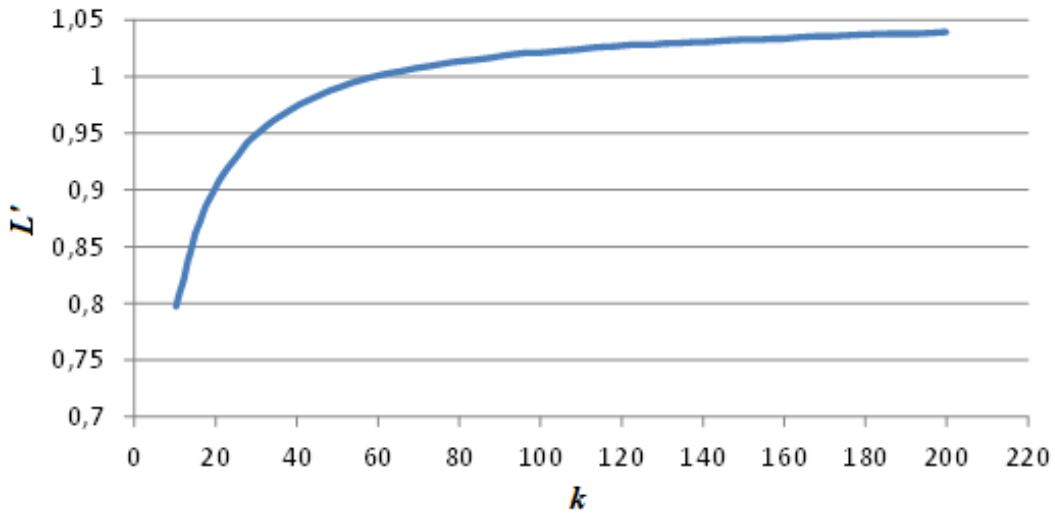


Figure 2. Variation of max (L') with k

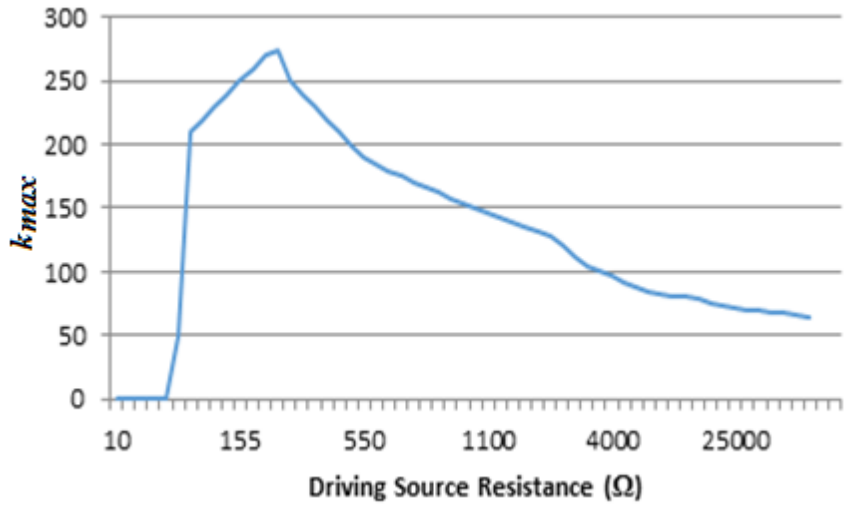


Figure 3. k_{max} with driving source resistance

Simulation results show that when $R_s << 1/g_{m1}$ the buffer is unstable for all values of C_s. As R_s becomes comparable to $1/g_{m1}$, the buffer is stable even when the driving source capacitance is as large as $275C_b$. Maximum value of C_s decreases as R_s increases further. A summary of the stability conditions for the test setup is given in *Table 2.*

Table 2. Circuit Stability Conditions ("-" represents don't care conditions)

L	R_s	C_s	L'	**Result**
< 1	-	-	< 1	Stable
=1.05	$\gg 1/g_{m1}$	-	> 1	Unstable
	$\ll 1/g_{m1}$	$\geq 65C_b$		
	$\cong 1/g_{m1}$	$\geq 275C_b$		
	$\gg 1/g_{m1}$	$\leq 65C_b$	< 1	Stable

As mentioned before, when the loop gain of the buffer is less than unity, buffer is unconditionally stable for any signal source. If the designer tries to design for minimum input resistance, loop gain must be designed as close to 1 as possible, but less than 1 for stability. If the buffer is designed to achieve a loop gain very close to 1 to minimize the input resistance, the actual loop gain might end up being larger than 1 after manufacturing due to environmental factors, and process variations and size mismatch. If loop gain of the buffer ends up being larger than 1 for any reason, circuit stability depends on the signal source.

In this study, a feedback control block as a bipolar current steering DAC is added to the buffer circuit to overcome this problem. The polarity bit selects whether current will be injected into or drawn from node C. The value of the current is set by a four bit current steering DAC. Feedback control block allows fine-tuning the loop gain. The value of the loop gain can be adjusted slightly smaller than 1 to minimize the input resistance and achieve stability.

The DAC modifies transconductance and channel resistance of M2. Since M1 and M3 are biased by a biasing current source, and the same current is mirrored to M4, the injected/drawn current does not change the transconductances and channel resistances of these transistors.

Tuning g_{m2} and g_{ds2} allows compensating for variations. Thus, this current control mechanism can adjust the input resistance by controlling L. This control mechanism also stabilizes an instable buffer by decreasing the loop gain. The circuit will be stable even when it is driven by sources with very low output resistances and very large capacitances.

To understand how the feedback control works, consider a buffer driven by a signal source with very small output resistance. If the circuit is stable, but has a large input resistance, this means 1-L(0) is positive, but not small enough. If L(0) is increased, input resistance will decrease. If g_{m2} decreases, L(0) increases. Therefore, current must be drawn from node C to decrease the bias current of M2. Polarity bit is set to 0 and the current drawn from node C is increased as long as the circuit is stable using the DAC. If the circuit is unstable, it means L(0)>1. This means L(0) must be decreased. Increasing g_{m2} will decrease L(0). Therefore, current must be injected to node C to increase the bias current of M2. Therefore, polarity bit is set to 1 and injected current is increased until the oscillation stops.

3. Proposed CCII circuit using the Positive Feedback Input Buffer

The second generation current conveyor (CCII) is indubitably the most popular current-mode building block, since its introduction in 1970 [17]. It is a versatile and flexible circuit element which can be used in analog circuit design for both linear and non-linear applications [6]. An ideal CCII has port relations given in (7). Ideal CCII has zero impedance at terminal X, infinite impedance at nodes Y and Z.

$$\begin{bmatrix} v_x \\ i_y \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \end{bmatrix} \tag{7}$$

The input resistance at terminal X can be decreased using negative feedback [10] or positive feedback [11,15]. In CCII design, class AB topologies are preferred at inputs to avoid limitation

of DC quiescent current, which also contributes positively to the better signal to noise ratios [18]. However, the input must have a well-defined DC quiescent current so that performance parameters of the circuit such as frequency response and power consumption do not change during operation. It had been shown that class AB current input stages with positive feedback can be designed with well-defined quiescent currents [16].

We propose a class AB fully differential CCII architecture that uses positive feedback along with negative feedback at the current input to achieve a very low input resistance. The amplifier used for negative feedback also provides the high input impedance needed for the voltage input. The proposed CCII is shown in *Figure 4*. The circuit has a very small impedance at node X, infinite impedance at node Y and very large impedance at output nodes Z+ and Z-. Gain boosted cascode mirrors are used at the output nodes to achieve very high output impedance.

Transistors M9 and M12 are current sources biasing the input stage. VBP and VBN voltages are generated by biaing transistors Mb1-Mb3. M1-M4 constitutes a translinear loop; M1, M3, M10, and M11 also creates a second translinear loop. Thus, DC bias current through all transistors in both loops is determined by M9 and M12. Source voltages of M2, M4, M10, and M11 are approximately equal to the voltage of X. The simple differential amplifier force the voltage of X to be approximately equal to the voltage of Y.

M10 and M11 have a constant biasing current, so their gate-source voltage difference is

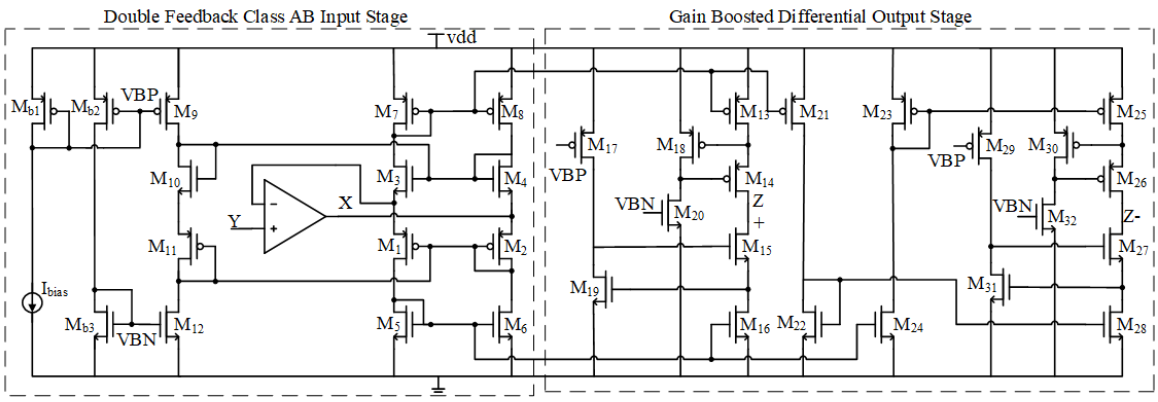


Figure 4. Proposed second generation current conveyor (CCII)

constant during operation. Sources of M1-M4 are held at approximately V_y by the feedback amplifier. However, gate-source voltage differences of M1-M4 increase or decrease when their drain currents change. When current is injected into node X, drain current of M1 increases. Therefore, its gate voltage decreases. Since drain currents of M10 and M11 are constant, gate voltage of M10 and M3 will also decrease. Thus, Drain currents of M3 and M7 will be less than M1 and M5. Current positive feedback loop formed by M3-M7-M8-M4 forces drain currents of M4 and M3 to be equal. The loop formed by M1-M5-M6-M2 forces drain currents of M1 and M2 to be equal. These currents are mirrored to the outputs and their difference is the output current. When current is drawn from node X, gate voltages of M10 and M11 increases and currents change accordingly. The circuit has a low DC quiescent power but can sink or source very large currents to/from node Z.

In Table 3, transistor dimensions for CCII and biasing circuit are given. For CCII and the biasing circuit, all channel lengths are selected as 1μm except for M39, which has a long channel of 20μm. Biasing current for current conveyor is selected as 10μA. Due to its class AB operation, there is no dynamic range limitation that is desired for low power operations.

Table 3. Transistor Dimensions for CCII

Transistor	W(μm)
Mb1, Mb2, M1,2,7,8,9,11,13,14,21,22,25,26	30
Mb3, M3,4,5,6,10,12,15,16,23,24,27,28	10
M17,18,29,30	6
M19,20,31,32	2

4. Filter Realization

Proposed CCII circuit was tested in filter applications reported in [19] as shown in *Figure 5*. Low pass, band pass, and high pass filter responses are observed at output 1, 2, and 3 respectively [19]. Transfer functions for the outputs are given in (8) and center frequency is given in (9).

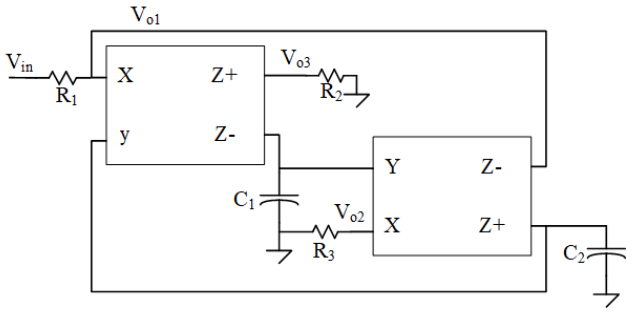


Figure 5. Voltage mode multifunction filter [19]

$$\frac{V_{o1}}{V_{in}} = \frac{G_1G_2G_3}{\Delta} \qquad \frac{V_{o2}}{V_{in}} = \frac{sG_1G_2G_3}{\Delta} \qquad \frac{V_{o3}}{V_{in}} = \frac{-s^2G_1G_2G_3}{\Delta} \tag{8}$$

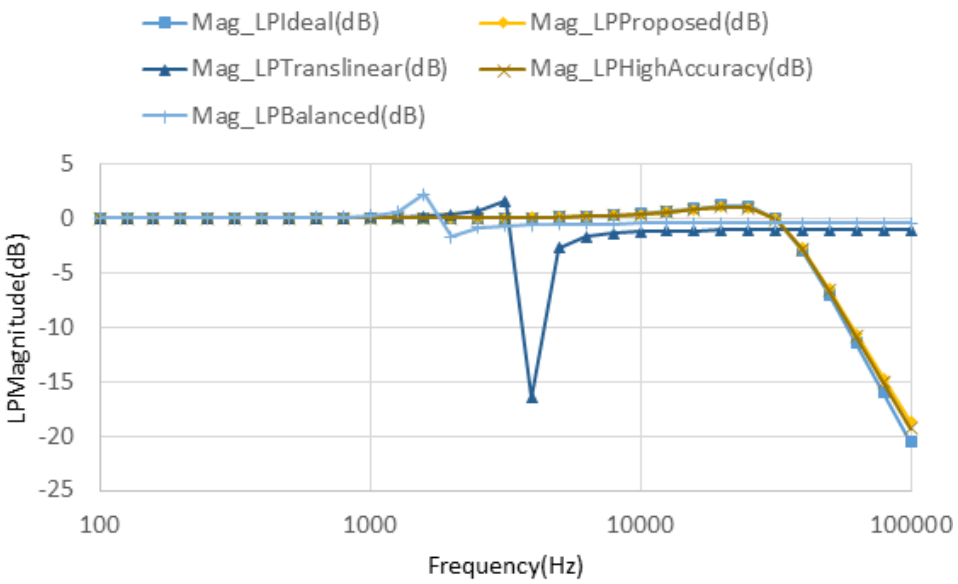
where $\Delta = s^2C_1C_2G_2 + sC_1G_2G_3 + G_1G_2G_3$.

$$\omega_0 = \sqrt{1/R_1R_3C_1C_2} \tag{9}$$

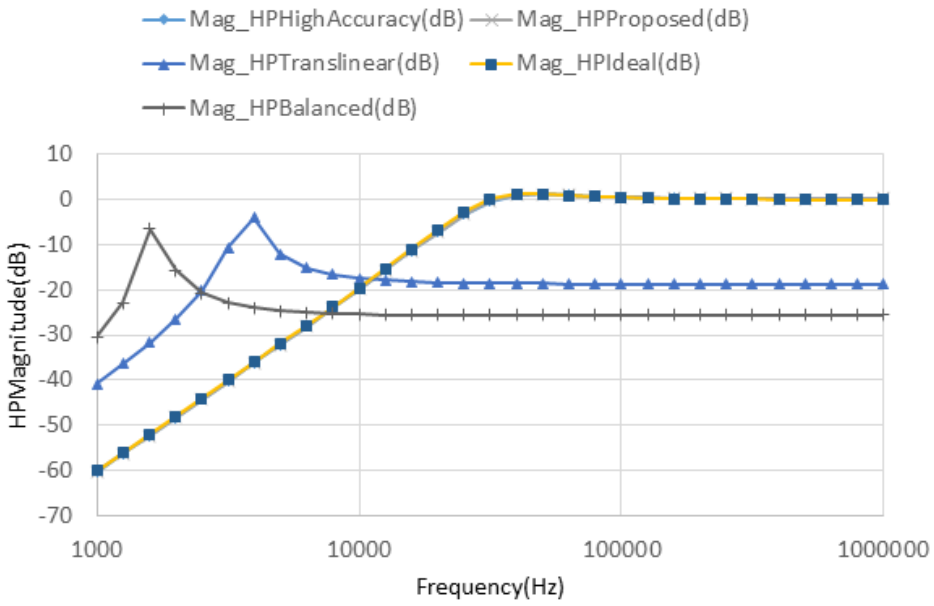
A CCII having near ideal characteristics is required for this filter topology since a high input impedance at terminal X degrades its performance. The filter in *Figure 5* is built with ideal CCII, the proposed CCII, translinear CCII, balanced differential CCII [20], and high accuracy CMOS current conveyor [21]. Performance of the filters were compared with AC simulations. Simulation results are shown in *Figure 6*. All current conveyors have same transistor sizes and bias currents for fair comparison. All resistors are 500Ω and all capacitors are 10nF, which corresponds to 32 kHz center frequency. This frequency is suitable for ultrasonic applications. Of course, filters with higher center frequency beyond 1MHz could be implemented with the proposed CCII, considering its bandwidth obtained from both simulations and measurements. However, this topology was picked for demonstrating the importance of low input impedance.

Figure 6 shows that filter characteristics for the proposed CCII and high accuracy CCII [21] are nearly identical to ideal CCII since their impedances at node X,Y and Z are nearly ideal. However, translinear CCII and balanced differential CCII are far from ideal filter characteristics

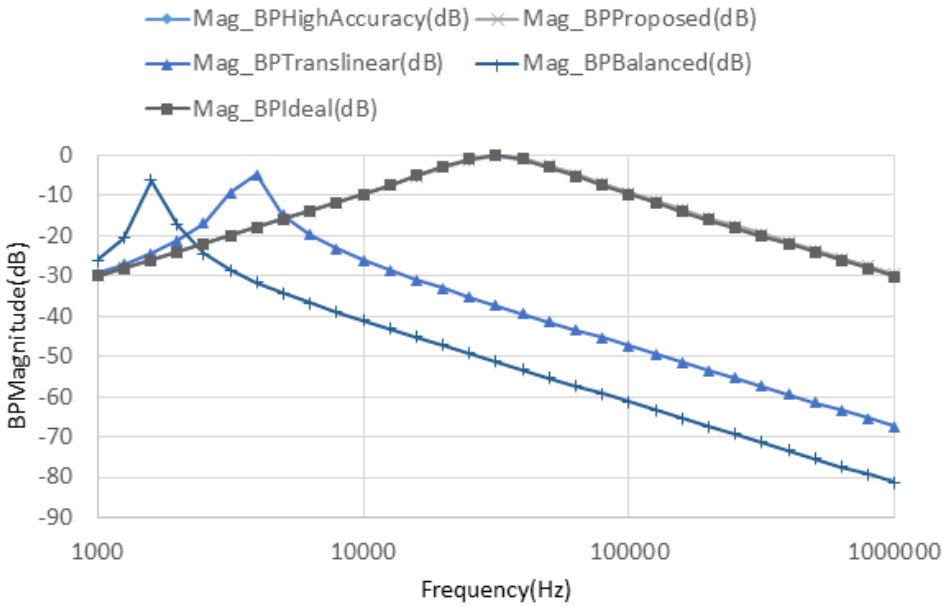
due to their relatively high impedance at node X. The advantage of the proposed CCII over high accuracy CCII is its class AB operation. High accuracy CCII suffers from restricted dynamic range due to bias circuit. *Figure 7* shows how the two structures perform when input current changes form -50µA to 50µA. Z node of the high accuracy CCII operates as a Class A output device due to limitation in tail current of differential amplifier. On the other hand, Z node for the proposed CCII operates as a Class AB device.



(a)



(b)



(c)

Figure 6. Magnitude responses of compared CCII structures: (a) Low pass filter, (b) High pass filter, (c) Band pass filter

Balanced differential CCII and translinear CCII have relatively high impedances at node X, which gives non-ideal filter characteristics, especially when using relatively low resistance values in filter application. High accuracy CCII has good performance on filter characteristics; however it suffers from limited bias current. We propose a class AB CCII structure, has a nearly zero impedance at node X and very large impedances at node Y and Z. It is a big advantage for low noise, low power ultrasonic applications.

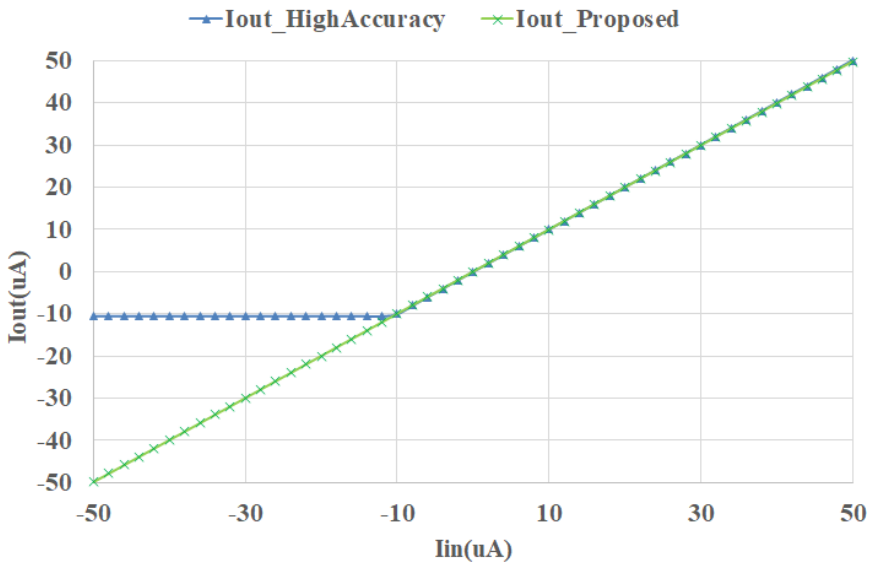
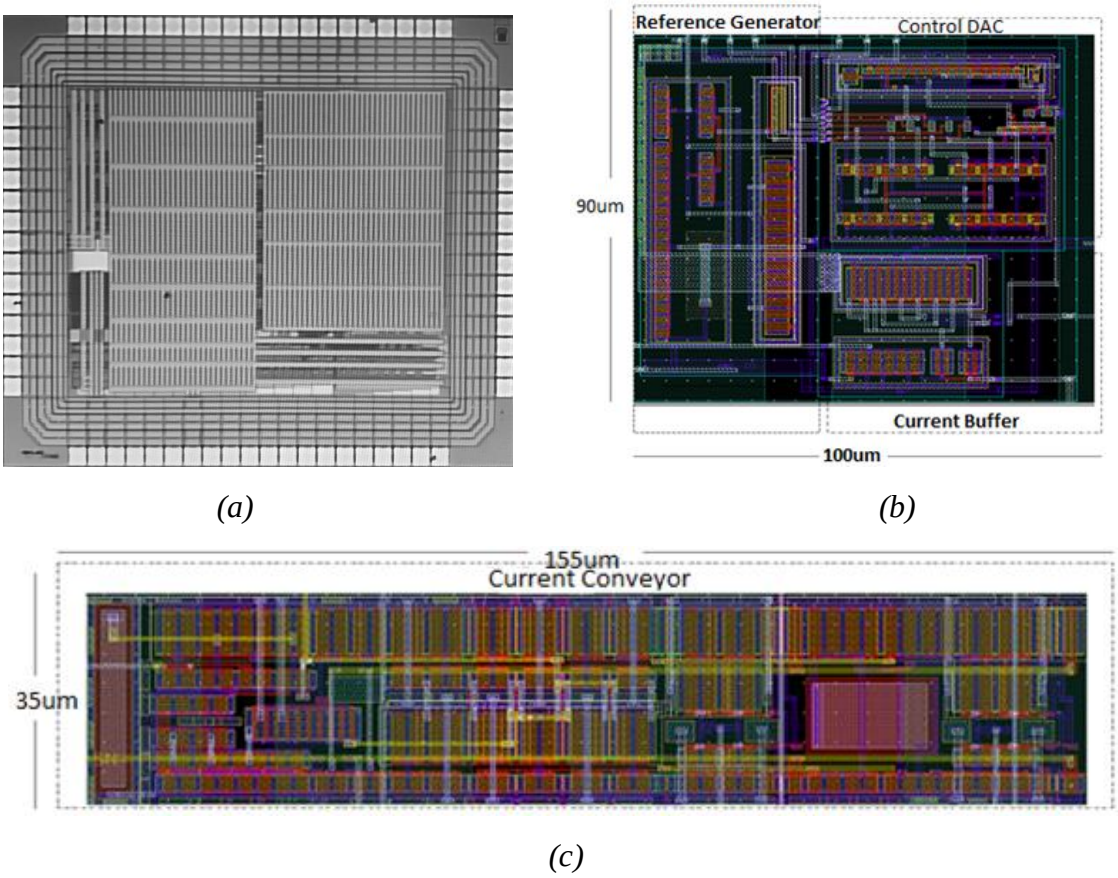


Figure 7. Current transfer characteristics of the proposed CCII and high accuracy CCII

5. Measurement Results and Discussion

We fabricated our design in AMS 2P4M 0.35µm process. Chip micrograph of the fabricated test devices, and their layouts are given in *Figure 8*. The areas of the proposed current conveyor and buffer are 155µm x 35µm and 90µm x 100µm (with control DAC and reference generator), respectively. Total chip area is 0.144 m^2.



(a) *(b)*

(c)

Figure 8. Fabricated chip (a) micrograph of the fabricated test devices, (b) layout of the proposed current buffer, and (c) layout of the proposed CCII

Test setup for input resistance measurement is given in *Figure 9*. Voltage signal from function generator were converted to current with LM13700 OTA. Input resistance of buffer is measured using a current divider setup. R_{test} is a 10 Ω resistor. We didn't place any AC ammeters in series with R_{test} nor the input of buffer to avoid adding resistances to these paths. Coupling capacitor isolates DC bias point of OTA output and current buffer input. The current output of the OTA

and the current output of M5 in the input buffer were compared in order to figure out the input resistance. Input resistance was measured for 5 test chips. Measurement results are summarized in *Table 4.* We initially observed oscillation for 2 chips. Therefore, we injected current into M2 to increase g_{m2}. Current injection can be activated setting the polarity bit to 1. For 3 chips, initial resistances were larger than R_{test} and we have drawn current from node C to decrease g_{m2} and increase loop gain. In both cases we brought L to a value very close to, but less than 1. Better results can be achieved if a higher resolution current steering DAC is used.

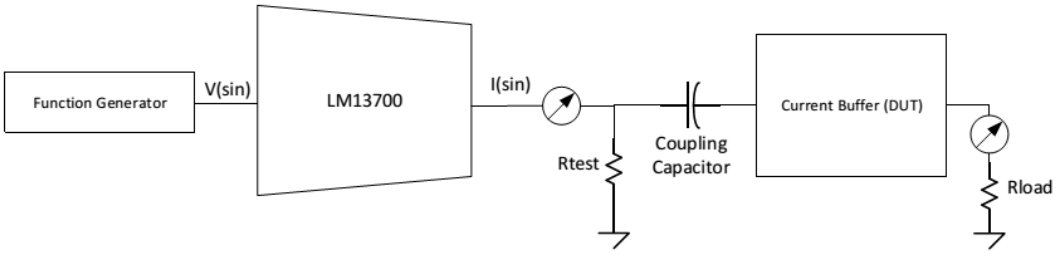


Figure 9. Test setup for measuring impedance of buffer

Table 4. Measurement Results for Input Resistance and Required Control Bits for Calibration

	Initial Input Resistance	**Calibration Code**	**Input Resistance with Calibration**
Chip 1	$R_{in} < 0$	0001, b_p=1	$R_{in} \cong 0$
Chip 2	$R_{in} < 0$	0011, b_p=1	$R_{in} \cong 0$
Chip 3	$R_{in} \cong$20ohm	0100, b_p=0	$R_{in} \cong 0$
Chip 4	$R_{in} \cong$100 ohm	0111, b_p=0	$R_{in} \cong 0$
Chip 5	$R_{in} \cong$20 ohm	0100, b_p=0	$R_{in} \cong 0$

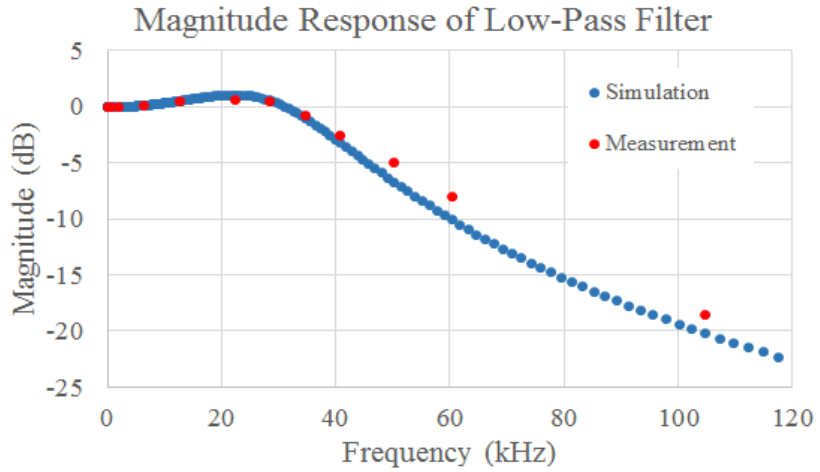
Measurement results, given in *Table 5*, reveal that the proposed fully differential CCII circuit has infinite impedance at node Y at DC frequencies, and it is larger than 1MΩ at 5 MHz. Node Z has very high impedance (230 GΩ) at DC frequencies and it is larger than 1MΩ at 5MHz. Impedance at X is approximately equal to 5Ω for low frequencies and it is lower than 50Ω at 5 MHz. The circuit has a current gain (I_z/I_x) value of 1.005 for Z+ and Z- outputs. 3dB frequency

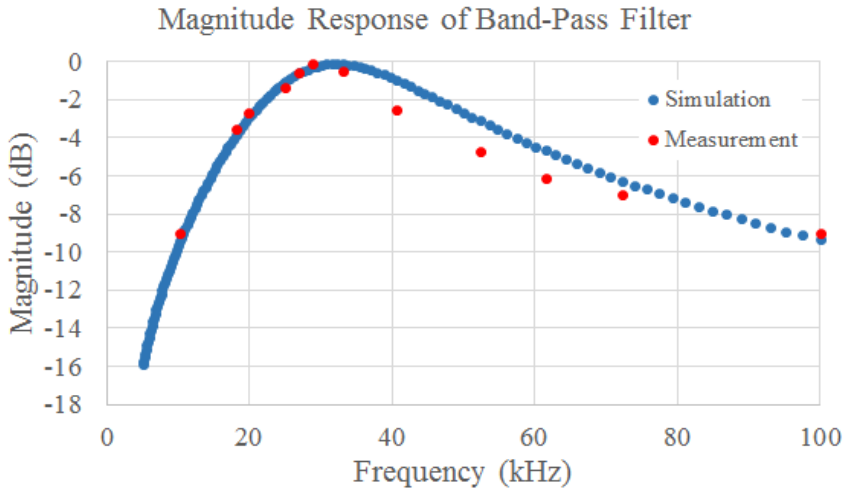
for X to Z transfer function is approximately 20 MHz, and ratio of V_x and V_y is 0.96 at DC and it has a bandwidth of approximately 50Mhz. As a summary of *Table 5*, we can claim that the proposed fully differential current conveyor demonstrates nearly ideal CCII properties.

Measurement results for low-pass, high-pass and band-pass filters built with the filter topology in *Figure 5* are shown in *Figure 10*. Simulated and measurement results for filter circuits also show that the proposed CCII has nearly ideal characteristics.

Table 5. Measurement Results for the Proposed Fully Differential CCII

Voltage Ratio (V_x/V_y) and bandwidth	0.96, 50MHz
Current Gain (I_z/I_x) and bandwidth	1.005, 20MHz
Impedance of Terminal Y	Very large @ DC , >1MΩ @ 5MHz
Impedance of Terminal X	5 Ω @ DC, <50 Ω @ 5MHz
Impedance of Terminal Z+ and Z-	230GΩ @DC, >1MΩ @ 5 MHz





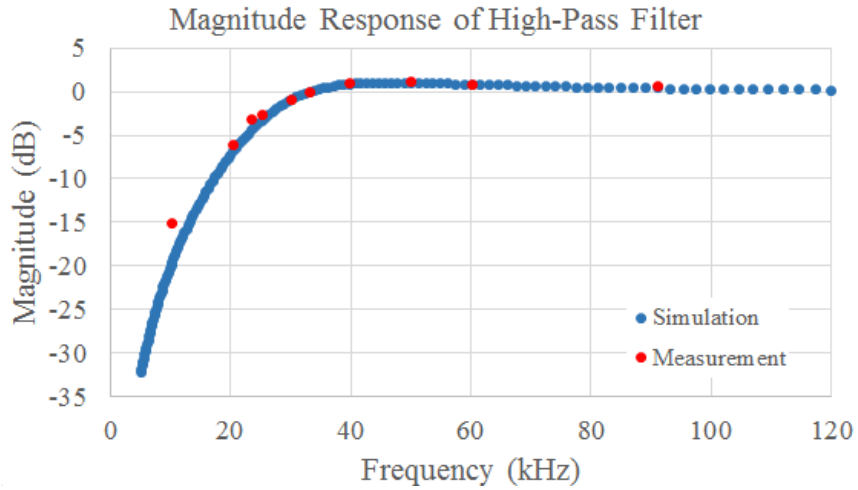


Figure 10. Magnitude response of filters realized with the proposed CCII circuit

6. Conclusion

This study has introduced a novel current input buffer that has a very low input resistance. The current buffer achieves low resistance using a positive feedback loop. Even though the buffer is potentially unstable because of positive feedback, a feedback control block assures stability while minimizing input resistance. The stability is guaranteed for all possible source capacitor and resistor values of the driving signal source as well as for process, mismatch, and environmental variations. A second-generation current conveyor (CCII) using this input buffer is also proposed. Measurements have verified that the input current buffer achieves very low input resistance. The proposed CCII built with the proposed current buffer is shown to have almost perfect current input terminal behavior. Test filter structures built using the proposed CCII perform close to filters simulated with ideal CCII. Although we explicitly show our the proposed current buffer in CCII applications, it can be used in any current input circuit including readout circuits of sensors with current mode outputs. Ideal current inputs can be realized using the proposed current buffer.

References

[1] Ripka P. Electric current sensors: a review. Meas Sci Technol 2010;21:112001. doi:10.1088/0957-0233/21/11/112001.

[2] Mantenuto P, Marcellis AD, Ferri G. Uncalibrated Analog Bridge-Based Interface for Wide-Range Resistive Sensor Estimation. IEEE Sens J 2012;12:1413–4. doi:10.1109/JSEN.2011.2172414.
[3] Liu M-C, Dai C-L, Chan C-H, Wu C-C. Manufacture of a Polyaniline Nanofiber Ammonia Sensor Integrated with a Readout Circuit Using the CMOS-MEMS Technique. Sensors 2009;9:869–80. doi:10.3390/s90200869.
[4] Toumazou C, Lidgey FJ, Haigh. Analogue IC Design: The Current-Mode Approach. IET Digital Library; 1993.
[5] Gilbert B. A new wide-band amplifier technique. IEEE J Solid-State Circuits 1968;3:353–65. doi:10.1109/JSSC.1968.1049924.
[6] Palmisano G, Palumbo G, Pennisi S. CMOS Current Amplifiers. Boston, MA: Springer US; 1999.
[7] Bajer J, Vavra J, Biolek D. A new building block for analog signal processing: current follower/inverter buffered transconductance amplifier. 2009 PhD Res. Microelectron. Electron., 2009, p. 136–9. doi:10.1109/RME.2009.5201325.
[8] Philipp RM, Orr D, Gruev V, Spiegel JV der, Etienne-Cummings R. Linear Current-Mode Active Pixel Sensor. IEEE J Solid-State Circuits 2007;42:2482–91. doi:10.1109/JSSC.2007.907168.
[9] Njuguna R, Gruev V. Linear current mode image sensor with focal plane spatial image processing. Proc. 2010 IEEE Int. Symp. Circuits Syst., 2010, p. 4265–8. doi:10.1109/ISCAS.2010.5537567.
[10] Abou-Allam E, El-Masry EI. A 200 MHz steered current operational amplifier in 1.2μm CMOS technology. IEEE J Solid-State Circuits 1997;32:245–9. doi:10.1109/4.551917.
[11] Smith KC, Sedra A. The current conveyor - A new circuit building block. Proc IEEE 1968;56:1368–9. doi:10.1109/PROC.1968.6591.
[12] Sedra AS. The current conveyor: history and progress. IEEE Int. Symp. Circuits Syst., 1989, p. 1567–71 vol.3. doi:10.1109/ISCAS.1989.100659.
[13] Temes GC, Ki WH. Fast CMOS current amplifier and buffer stage. Electron Lett 1987;23:696–7. doi:10.1049/el:19870495.
[14] Altun M, Kuntman H. Design of a fully differential current mode operational amplifier with improved input–output impedances and its filter applications. AEU - Int J Electron Commun 2008;62:239–44. doi:10.1016/j.aeue.2007.03.020.
[15] Wang Z. Wideband class AB (push-pull) current amplifier in CMOS technology. Electron Lett 1990;26:543–5. doi:10.1049/el:19900353.
[16] Altun M, Kuntman H. High CMRR current mode operational amplifier with a novel class AB input stage. Proc. 17th ACM Gt. Lakes Symp. VLSI, Stresa-Lago Maggiore, Italy: ACM; 2007, p. 192–5.
[17] Sedra A, Smith K. A second-generation current conveyor and its applications. IEEE Trans Circuit Theory 1970;17:132–4. doi:10.1109/TCT.1970.1083067.
[18] Bruun E. Analysis of the Noise Characteristics of CMOS Current Conveyors. Analog Integr Circuits Signal Process 1997;12:71–8. doi:10.1023/A:1013282902466.
[19] Chang C-M, Lee M-J. Voltage-mode multifunction filter with single input and three outputs using two compound current conveyors. IEEE Trans Circuits Syst Fundam Theory Appl 1999;46:1364–5. doi:10.1109/81.802827.
[20] Chaisricharoen R, Chipipop B, Sirinaovakul B. CMOS CCCII: Structures, characteristics, and considerations. AEU - Int J Electron Commun 2010;64:540–57. doi:10.1016/j.aeue.2009.03.009.
[21] Hassanein WS, Awad IA, Soliman AM. New high accuracy CMOS current conveyors. AEU - Int J Electron Commun 2005;59:384–91. doi:10.1016/j.aeue.2004.10.001.